

# Iris 14"/15" Schematics

## Braswell - M

2015-06-05

REV : A00

*DY : None Installed*

*DEBUG XDP: For CPU XDP Debug Port installed*

*Share/nonS: Share ROM or Non Share ROM*

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**Cover Page**

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Document Number

**Iris BSW**

Rev

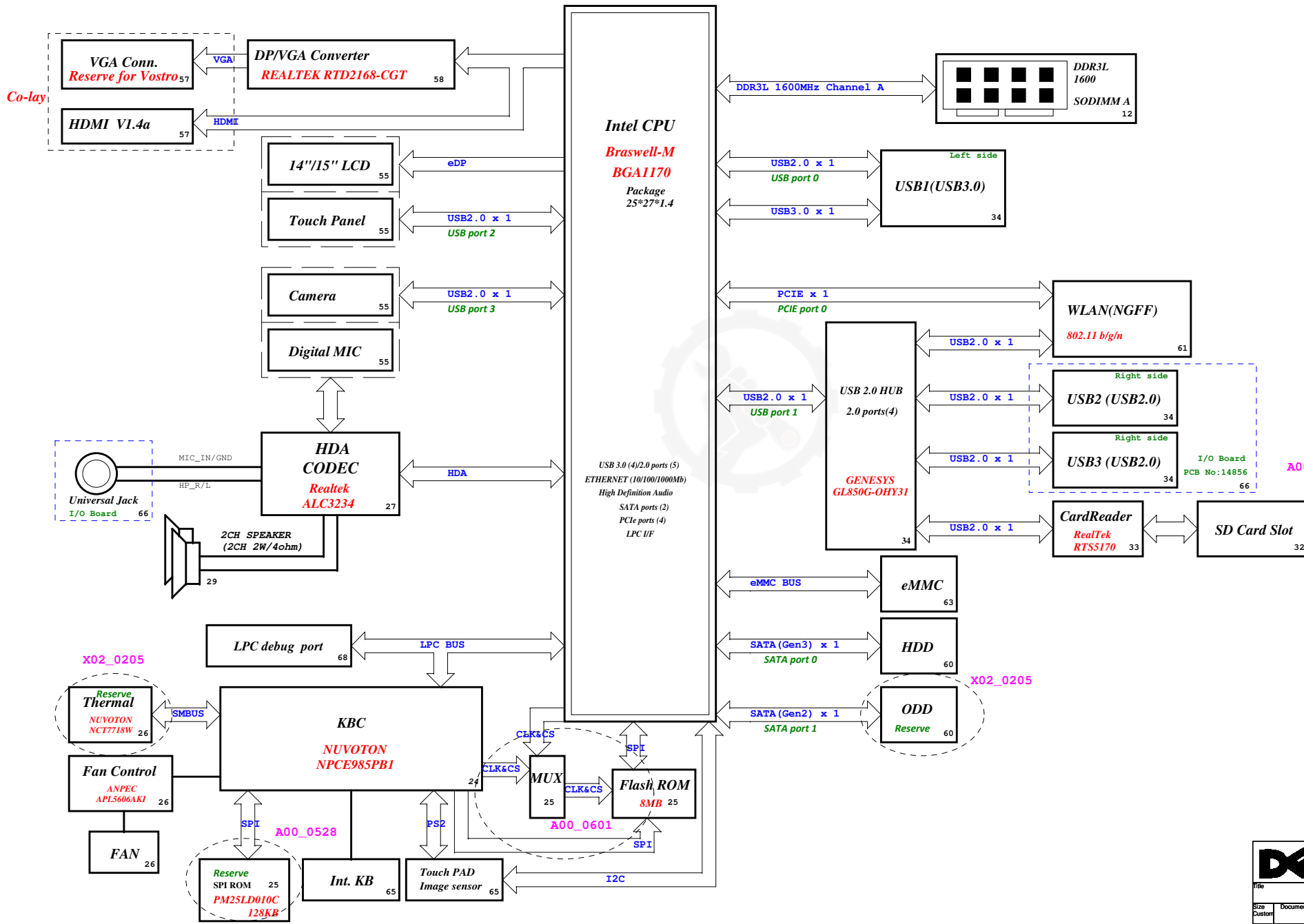
**A00**

Date: Thursday, June 04, 2015

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Project code:  
4PD03V010001  
PCB P/N: 896X3 A00\_0528  
PCB Number: 14279  
Revision: A00 A00\_0527

# Iris Braswell-M Block Diagram



CHARGER	
BQ24727RGRR-1-GP 44	
INPUTS	OUTPUTS
AD+	DCBATOUT
BT+	
SYSTEM DC/DC	
RT6576DGQW-GP 45	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5
CPU Core Power	
RT8171BGQW-GP 46, 47	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
GFX Core Power	
RT8171BGQW-GP 48	
INPUTS	OUTPUTS
DCBATOUT	GFX_CORE
DDR3L SUS	
TPS51716RUKR-GP 51	
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D675V_S0
CPU 1.05V	
SY8206DQNC-GP-U 50	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0
CPU 1.15V	
SYW232DFC-GP 50	
INPUTS	OUTPUTS
3D3V_S5	1D15V_S5
System LDO 1.8V	
SYW232DFC-GP 52	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5
System LDO 1.5V	
S-1339D15-M5001-GP 53	
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
System LDO 1.24V	
APL5930KAI 54	
INPUTS	OUTPUTS
1D8V_S5	1D24V_S5
System switches	
INPUTS	OUTPUTS
5V_S5	5V_S0
3D3V_S5	3D3V_S0
1D8V_S5	1D8V_S0
3D3V_S5	3D3V_S5_PRIME
PCB LAYER	
L1:Top L2:VCC L3:Signal L4:Signal L5:GND L6:Bottom	

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SSID = CPU

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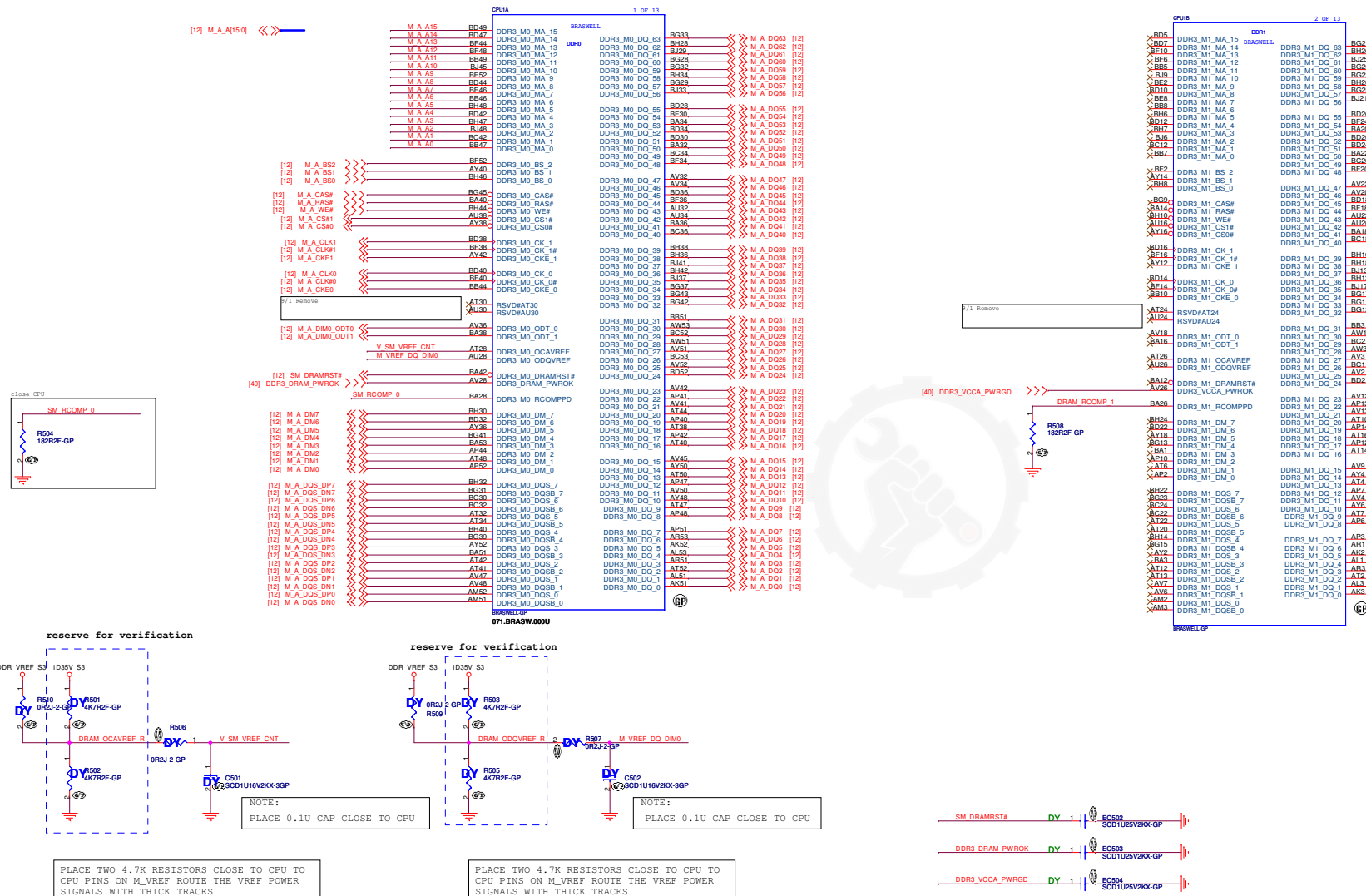
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Size  
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Document Number

Rev

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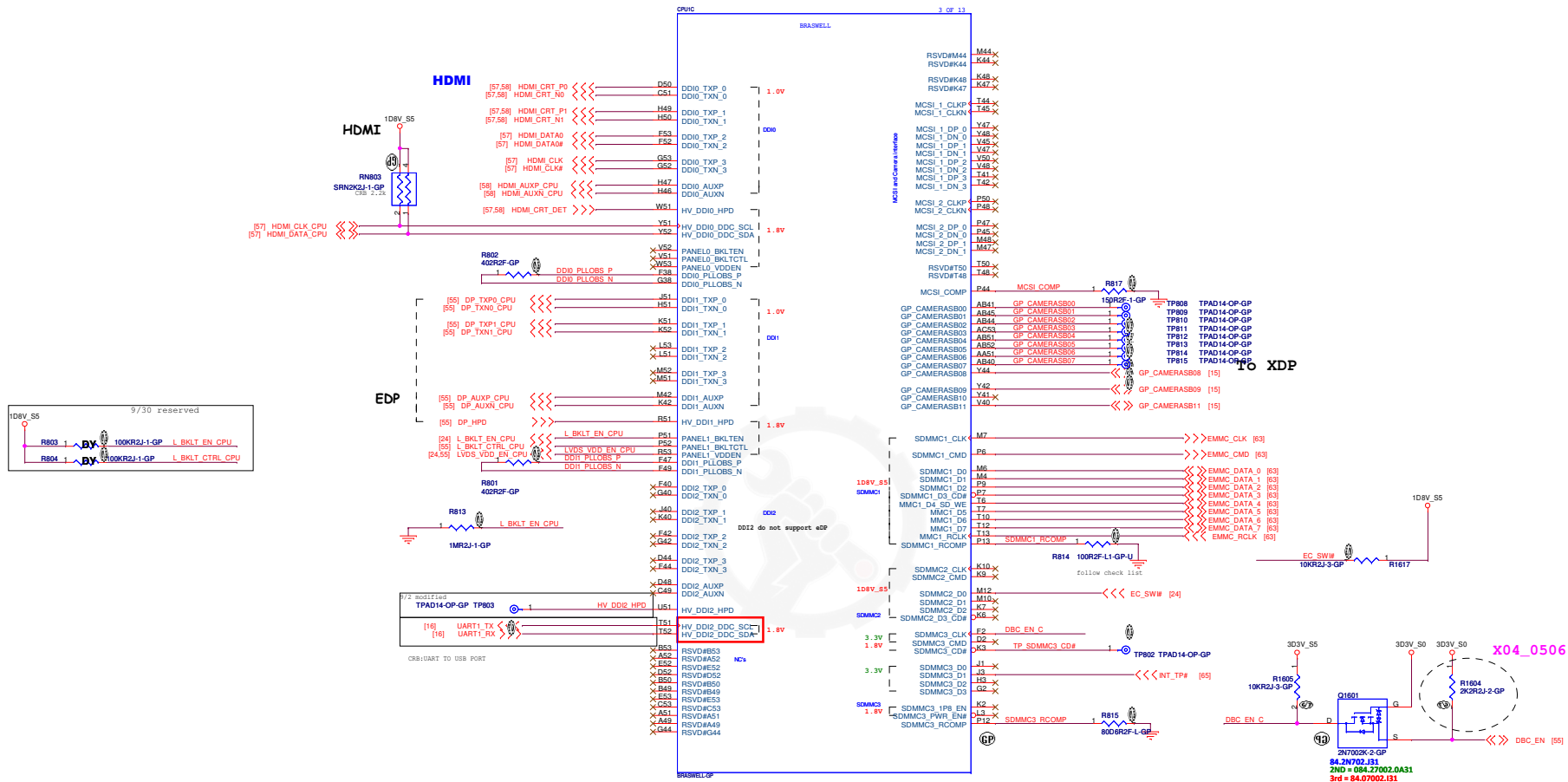
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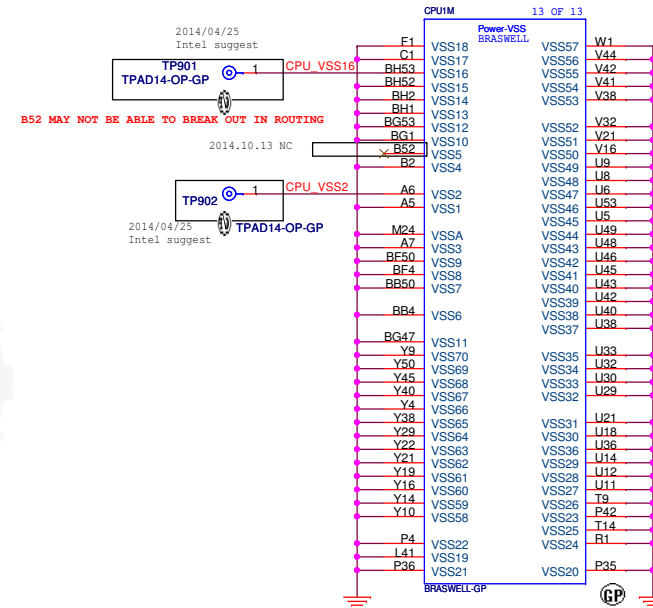
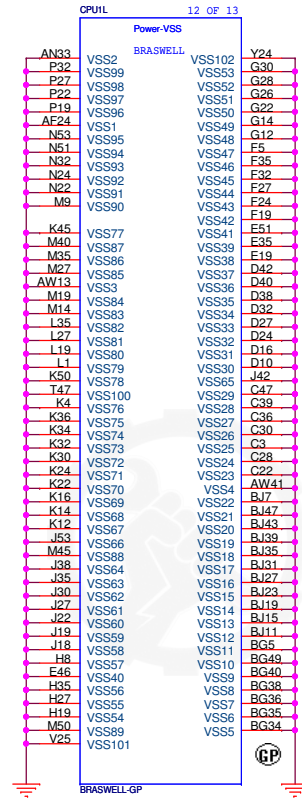
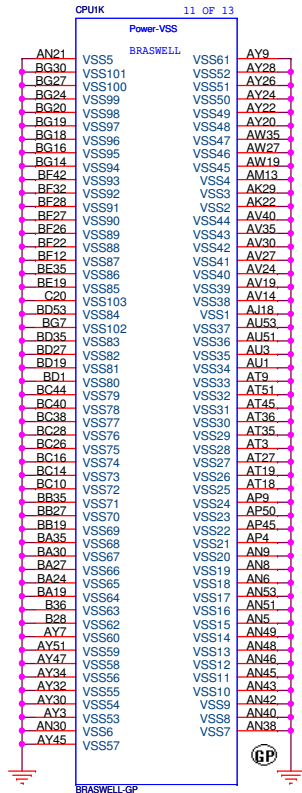
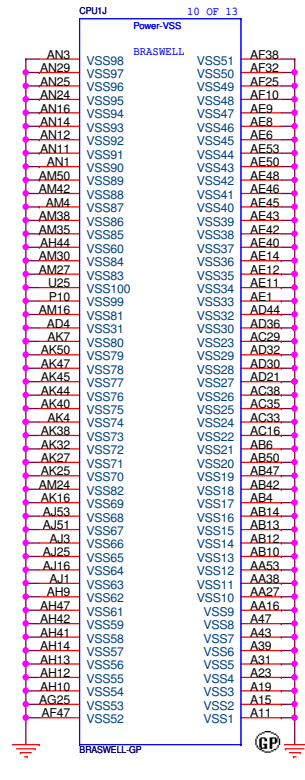
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SSID = CPU

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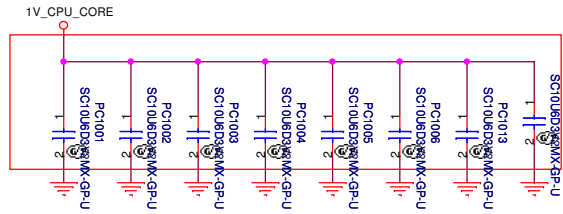
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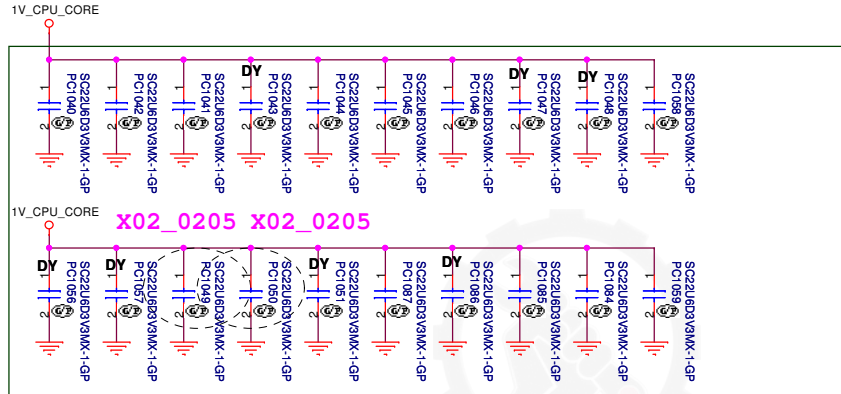
SSID = CPU

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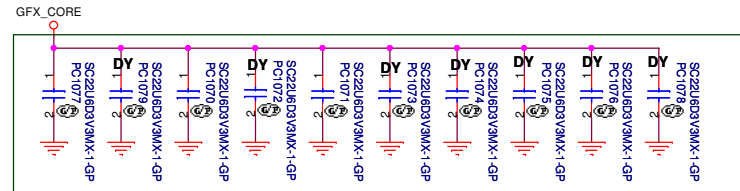
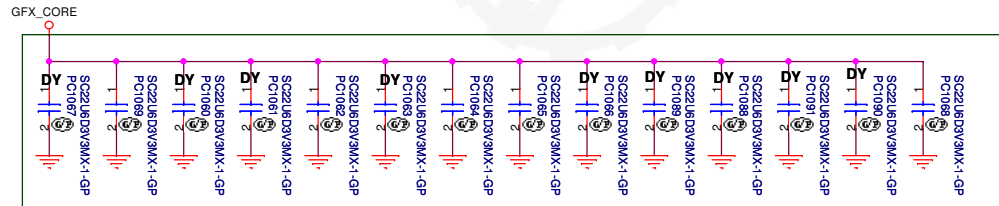
PLACE ALL THE CAPS  
UNDER THE PKG SHADOW



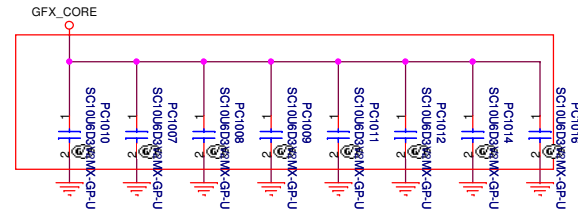
PLACE ALL THE CAPS  
NEAR BY PKG



PLACE ALL THE CAPS  
NEAR BY PKG



PLACE ALL THE CAPS  
UNDER THE PKG SHADOW

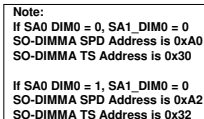


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9/10 Remove B1208-1213

9/10 Remove R1201 [Thermal Event]

DDR\_VREF\_S3

1035V\_S3

**Y**  
0R2J-2-GP  
R1213

**X04\_0513**

R120

R123

R124

R125

VREF\_DQ

VREF\_Q

C1213

080402-PAD

2CONUMM200

080402-PAD

reserve for verification

reserve for verification


SSID = MEMORY

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SSID = CPU


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SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC  
SHOULD BE PLACED OUTSIDE KOZ AREA

All the straps are sampled on the rising edge of the  
PMC\_RSMRST\_N signal (check list)

Description	DDI0_Detected	DDI1_Detected	A16 Swap Override	DSI Display Detected	Boot BIOS Strap BBS	Flash Descriptor Security Override	DFX Boot Halt Strap & VISA Early POSM Debug Enable	DFX Sus Debug Strap	ICLK, USB2, DDI SFR Supply Select	ICLK SFR Bypass	POSM Select	ICLK Xtal OSC Bypass	CCU SUS RO Bypass	RTC OSC Bypass
GPIO	GPIO_SUS0	GPIO_SUS1	GPIO_SUS2	GPIO_SUS3	GPIO_SUS4	GPIO_SUS5	GPIO_SUS6	GPIO_SUS7	SEC_GPIO_SUS8	SEC_GPIO_SUS9	SEC_GPIO_SUS10	GP_CAMERASB08	GP_CAMERASB09	GP_CAMERASB11
Schematic														
High	DDI0 Detect	DDI1 Detect	Normal Operation	DSI Detect	Boot from SPI	Weak internal pull-up Normal Operation	Normal	Weak internal pull-up Normal	1.35V	Weak internal pull-up Bypass with 1.05V	PMC	Bypass	Bypass	Bypass
Low	Disable	Disable	Change Boot Loader address (A16 Override)	Disable	Boot from LPC	Override	Halt boot enable	Sus Debug enable	1.25V	No bypass	Fuse controller	No bypass	No bypass	No bypass

Table 29. Straps (Sheet 1 of 2)

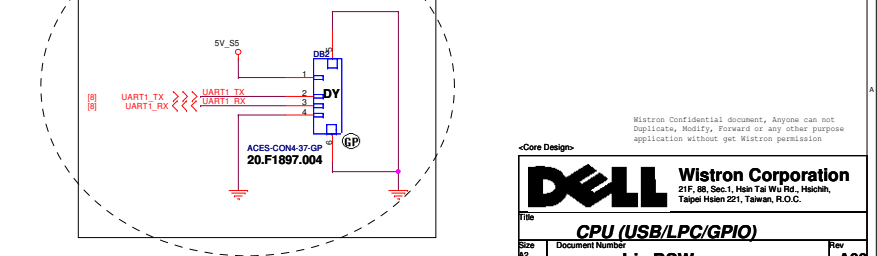
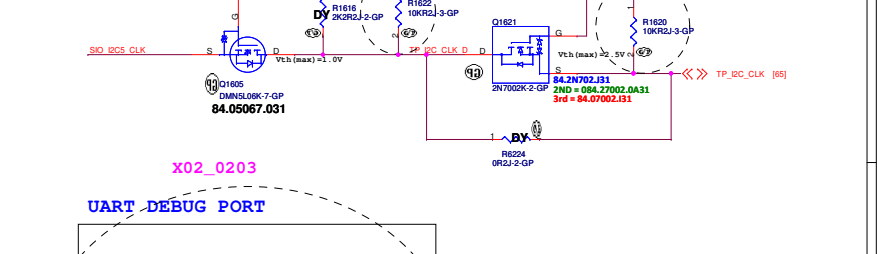
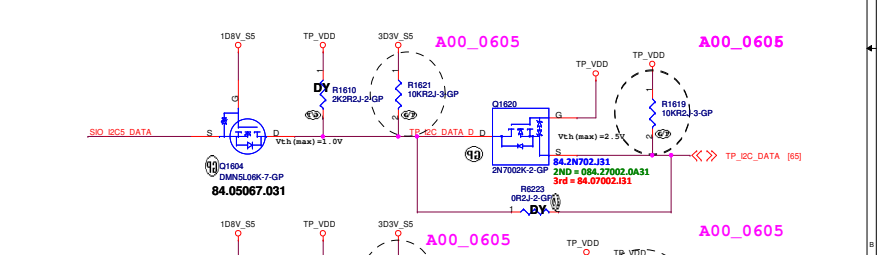
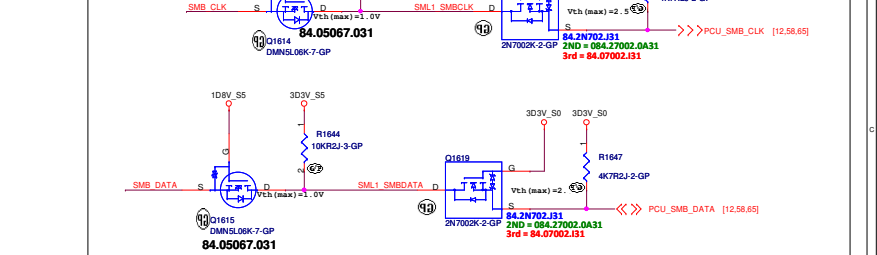
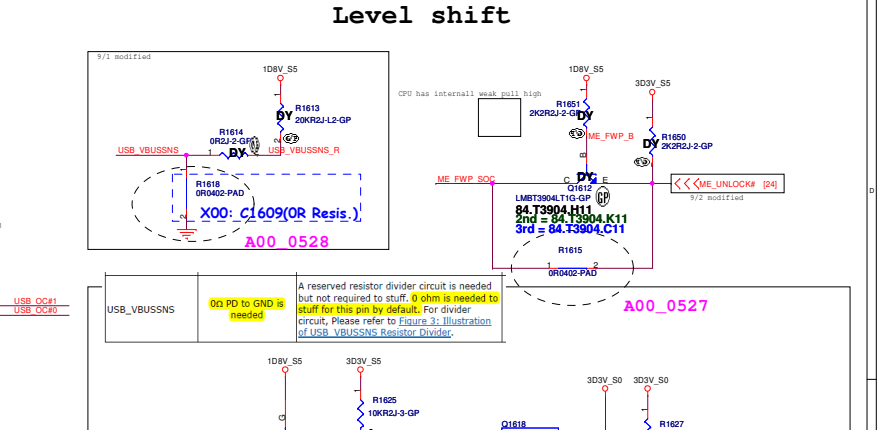
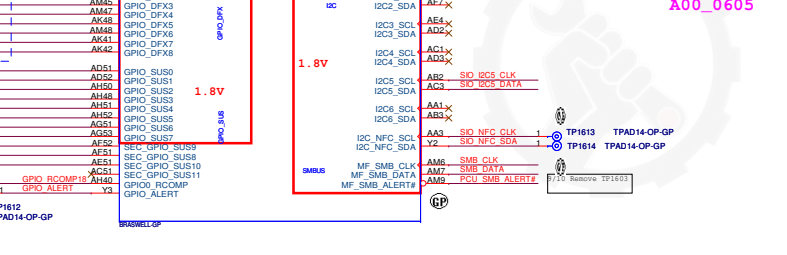
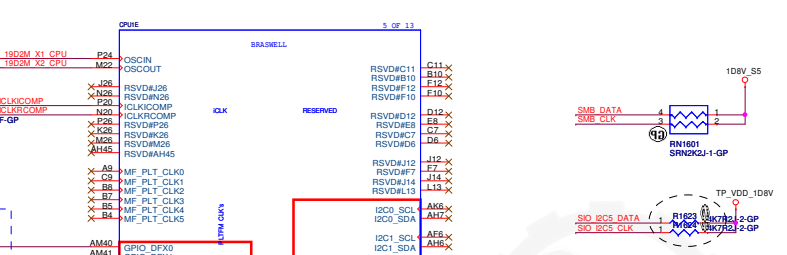
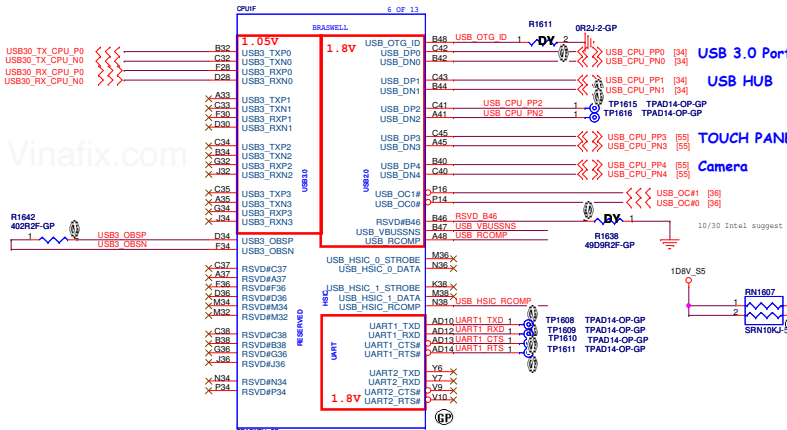
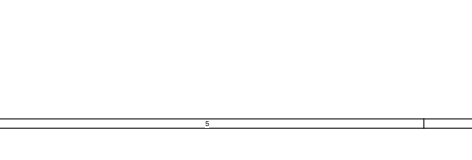
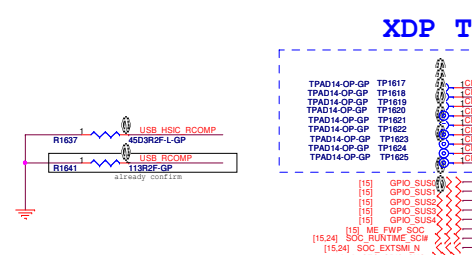
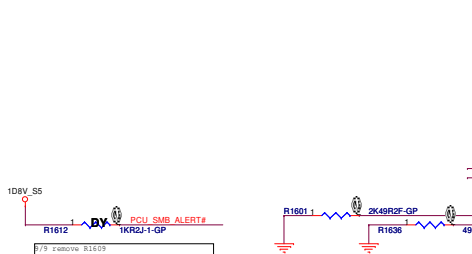
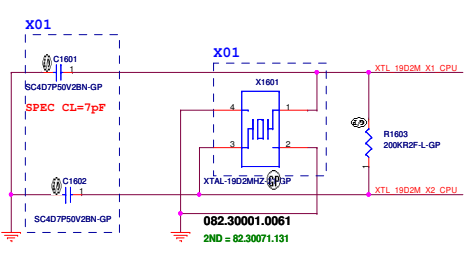
Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[0]	DDI0 Detect	Weak internal pull-down	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
GPIO_SUS[1]	DDI1 Detect	Weak internal pull-down	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS[2]	A16 swap override	Weak internal pull-up	Top Swap (A16 Override) 0 = Change Boot Loader address 1 = Normal Operation
GPIO_SUS[4]	Boot BIOS Strap BBS	Weak internal pull-up	BIOS Boot Selection 0 = - 1 = SPI
GPIO_SUS[5]	Flash Descriptor Security Override	Weak internal pull-up	Security Flash Descriptors 0 = Override 1 = Normal Operation

Table 29. Straps (Sheet 2 of 2)

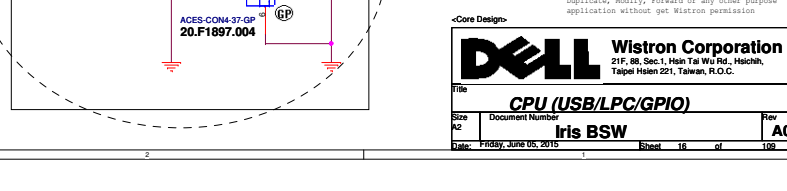
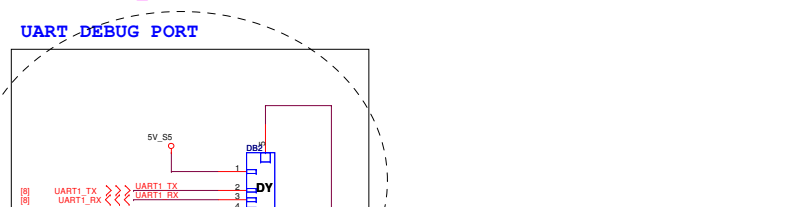
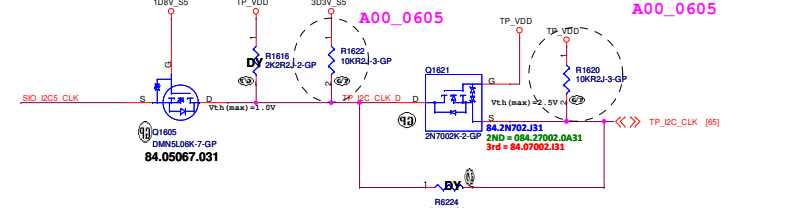
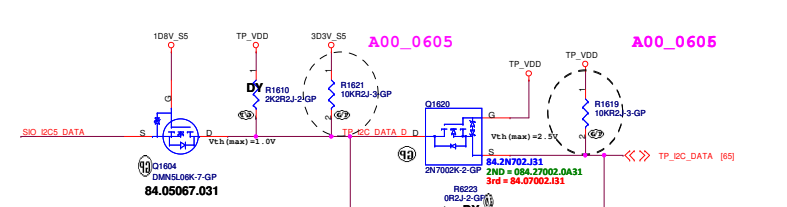
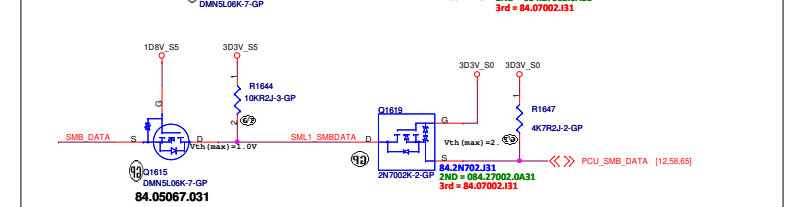
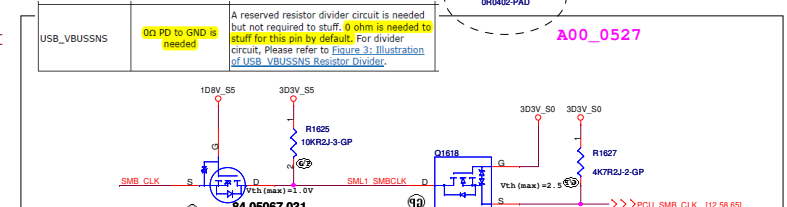
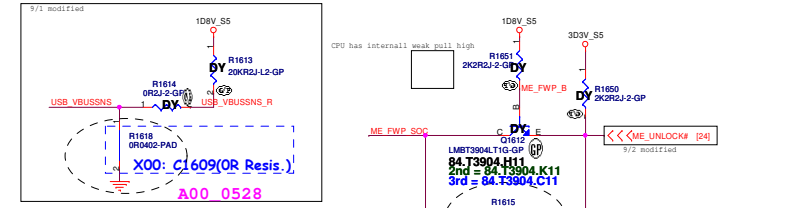
Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[8]	ICLK, USB2, DDI SFR Supply Select	Weak internal pull-down	0 = Supply is 1.25V 1 = Supply is 1.35V  This strap also contains PLL LDO 0: supply is 1.25V; 1: supply is 1.35V.  Selects supply voltage for LDOs used for PLLs, thermal oscillators, USB2, ICLK and DDI
GPIO_SUS[9]	ICLK, USB2, DDI SFR Bypass	Weak internal pull-up	0 = No bypass 1 = Bypass with 1.05V
GPIO_SUS[10]	POSM Select	Weak internal pull-down	Selects which POSM will be observed at time 0 0 = Fuse controller 1 = PMC
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass

CHV Straps [CRB] -- strap detect @ RSMRST# assertion				
Purpose	CHV Pin Name (refer CHV symbol PIN)	PU/PD (internal - Weak)	Options	Default State on board?
DDI0 Detected	GPIO_SUS0	PD	1- DDI0 Detect, 0- Disable	High
DDI1 Detected	GPIO_SUS1	PD	1- DDI1 Detect, 0- Disable	High
A16 swap override	GPIO_SUS2	PU	1- Default, 0- A16 override	High
DSI Display Detected	GPIO_SUS3	PD	1- DSI detect, 0- Disable	Low
Boot BIOS Strap BBS	GPIO_SUS4	PU	1- Boot from SPI, 0- Boot from LPC	High
Flash Descriptor Security Override	GPIO_SUS5	PU	1- Security enabled, 0- Security disabled	High
DFX Boot Halt Strap & VISA Early POSM Debug Enable	GPIO_SUS6	PU	1- normal, 0- Halt boot enable	High
DFX Sus Debug Strap	GPIO_SUS7	PU	1- Normal, 0- Sus Debug enable	High
ICLK, USB2, DDI SFR Supply Select	SEC_GPIO_SUS8	PU	1- 1.35V, 0- 1.25V	Low
ICLK SFR Bypass	SEC_GPIO_SUS9	PD	1- Bypass with 1.05V, 0- No Bypass	Low
POSM Select	SEC_GPIO_SUS10	PD	1- PMC, 0- Fuse controller	Don't care, if GPIO_SUS6 is pulled high.
ICLK Xtal OSC Bypass	GP_CAMERASB08	PD	1- Bypass, 0- No bypass	Low
CCU SUS RO Bypass	GP_CAMERASB09	PD	1- Bypass, 0- No bypass	Low
RTC OSC Bypass	GP_CAMERASB11	PD	1- Bypass, 0- No bypass	Low

SSID = PCH



Level shift






SSID = CPU

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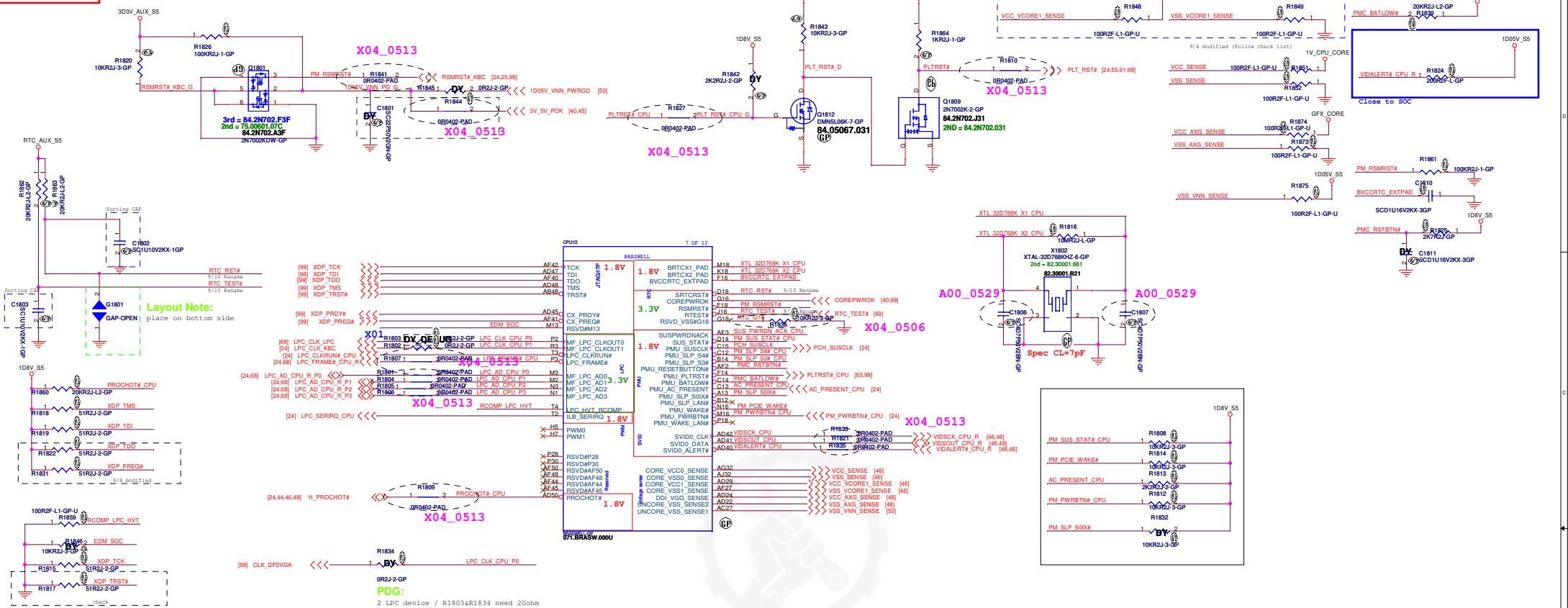
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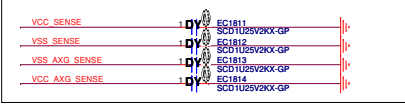
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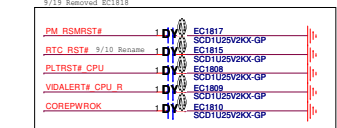
SSID = PCH



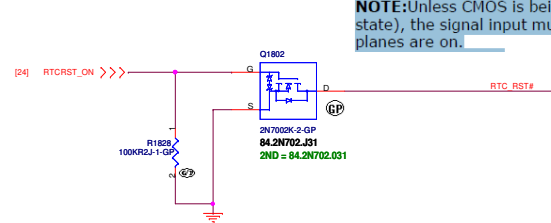
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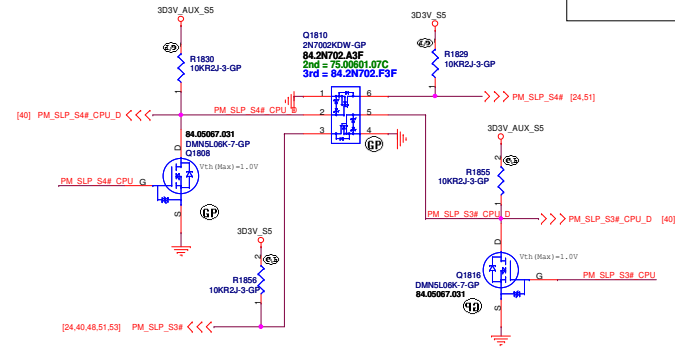
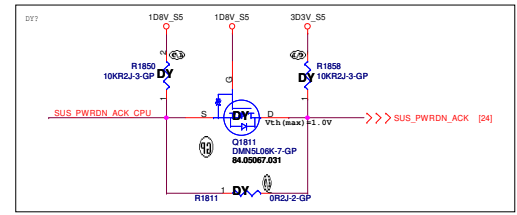
reserve the 0402 0.1u caps on reset for EMI.



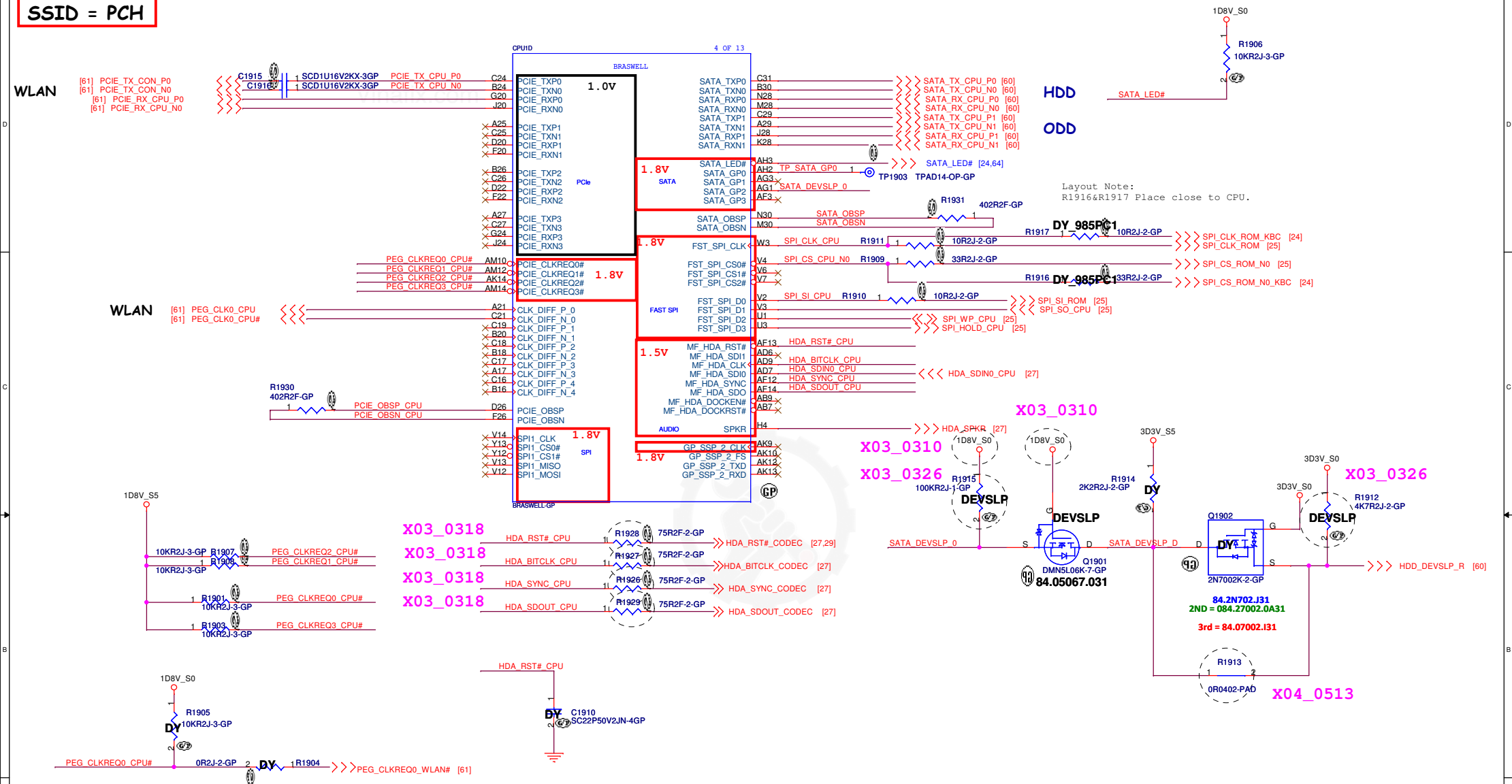
### RTC Reset



NOTE: Unless CMOS is being cleared (only to be done in the G3 power state), the signal input must always be high when all other RTC power planes are on.



**SSID = PCH**



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Title

**CPU (SATA/PCIE/IHDA)**

Size

Document Number

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SSID = PCH


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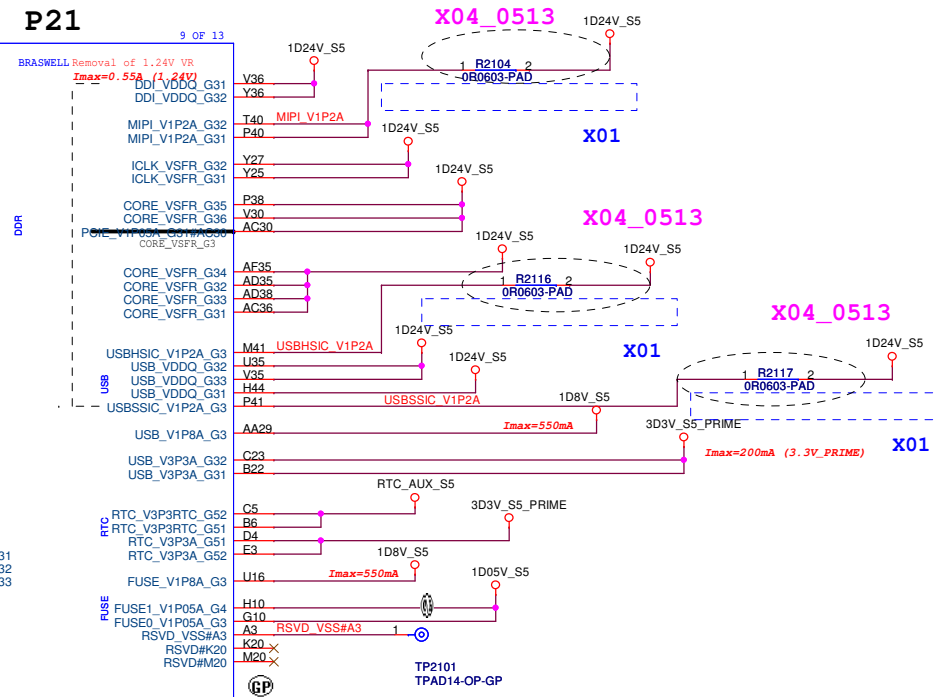
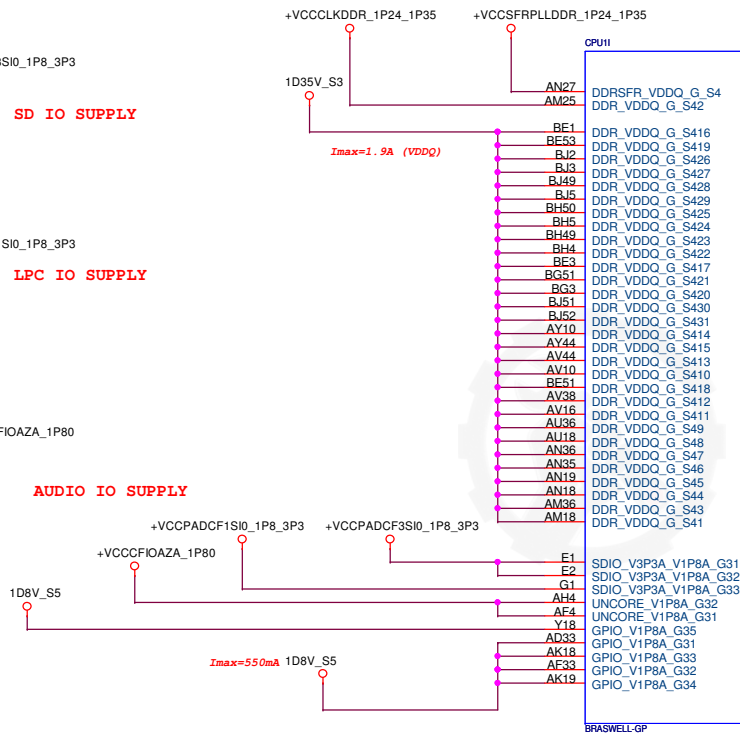
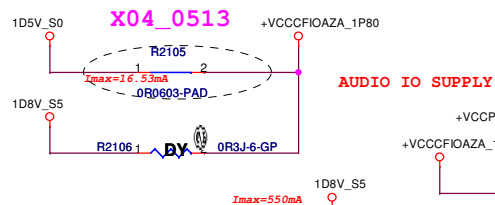
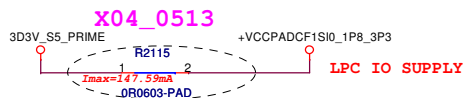
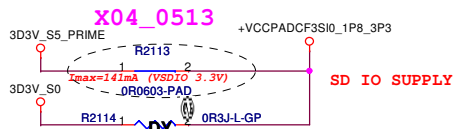
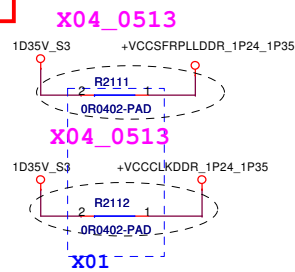


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**SSID = CPU**



When SSIC, HSIC, and CSI interface is not used, the following pins can be connected to ground: CSI (T40, P40), USB HSIC (M41), USB SSIC (P41).

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Title

**CPU (POWER1)**

Size

Document Number

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Date \_\_\_\_\_

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ev

Main Func = PCH

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Date: Thursday, May 28, 2015		Sheet 22 of	109


Main Func = PCH

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# Blanking



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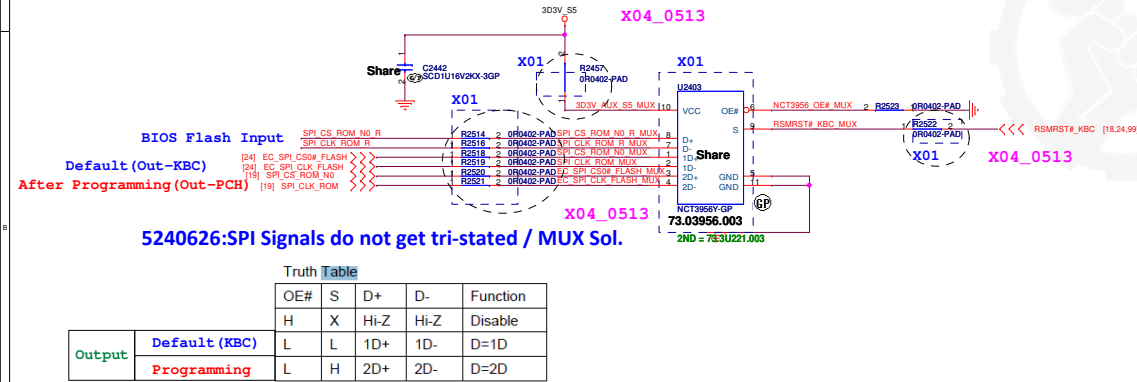
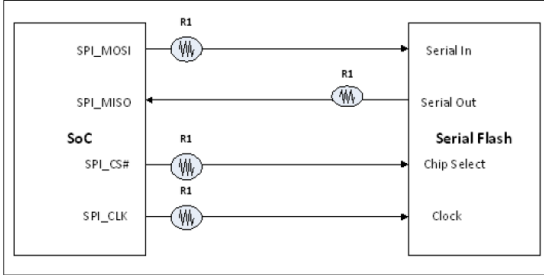
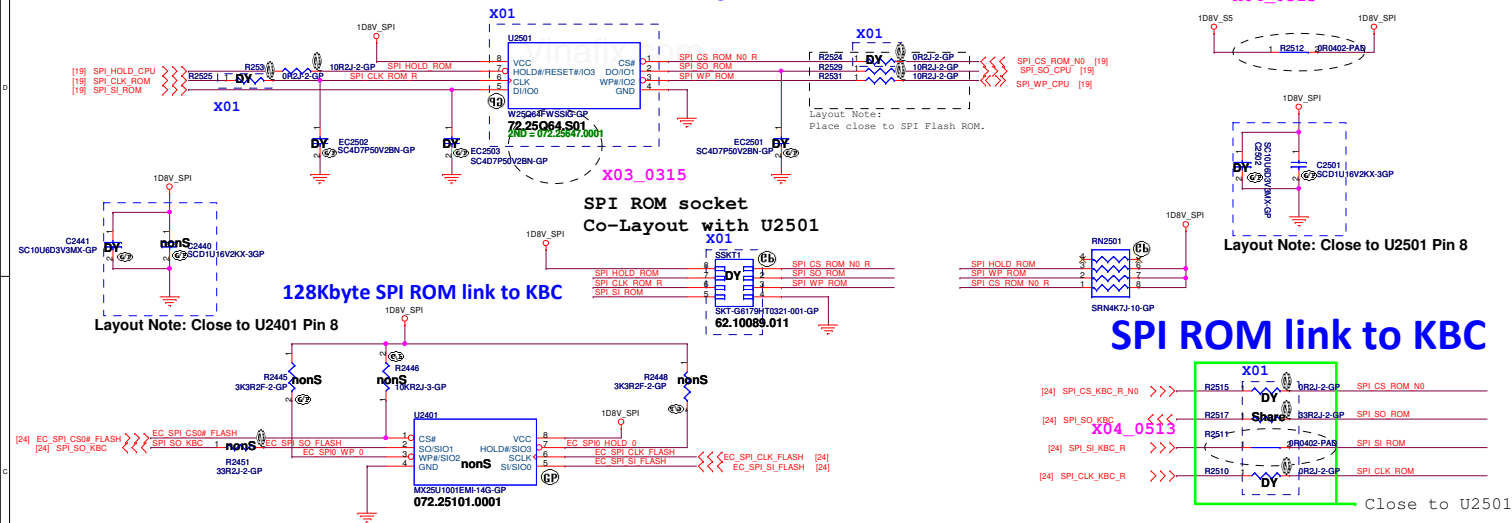
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)</b>			
Size A4	Document Number <b>Iris BSW</b>		Rev <b>A00</b>
Date: Thursday, May 28, 2015		Sheet 23 of	109





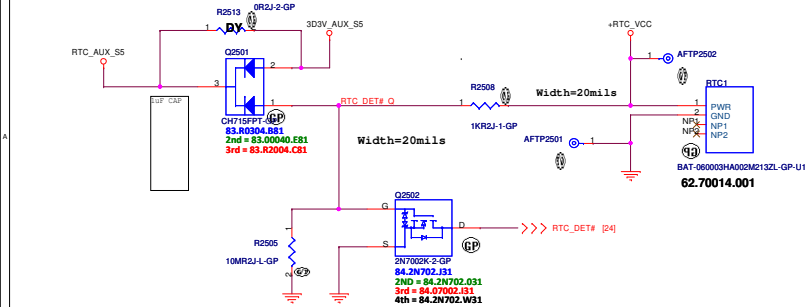
SSID = Flash.ROM

# SPI FLASH ROM (8M byte) for CPU



SSID = RTC

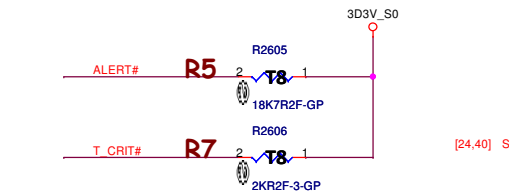
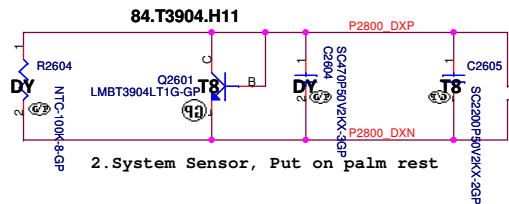
RTC coin cell  
23.20068.001



Main Func = Thermal Sensor

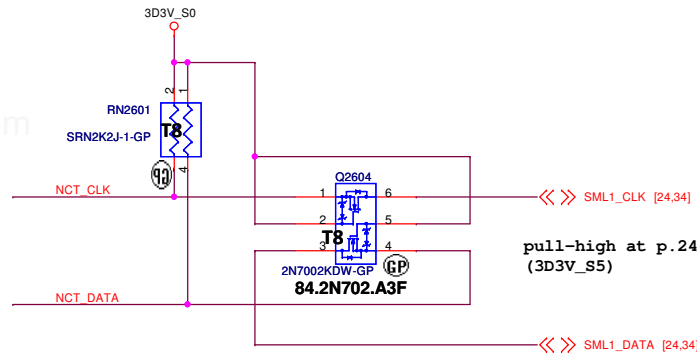
EE Note:  
1. PURE\_KBCT8: PURE\_HW\_SHUTDOWN# w/o through Q2603.  
2. T8: PURE\_HW\_SHUTDOWN# through Q2603.  
3. THM\_SENSOR: Thermal sensor NCT7718W solution.  
(Need to stuff R2601 and DY R2602 for THERM\_SYS\_SHDN#)

Layout notice :  
Both DXN and DXP routing 10 mil  
trace width and 10 mil spacing.

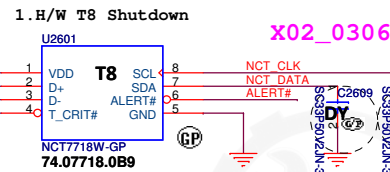


The default value is trapping after power up 100ms by different pull-up resistors of T\_CRIT# and ALERT# pin:

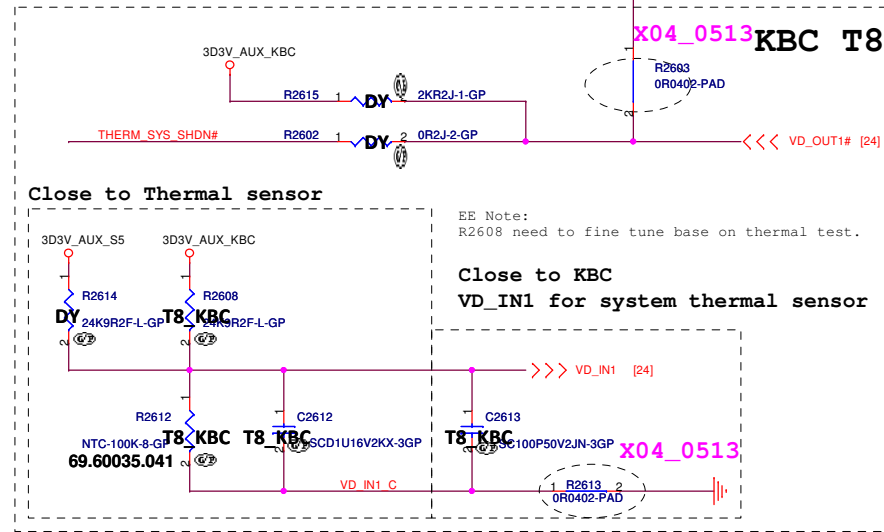
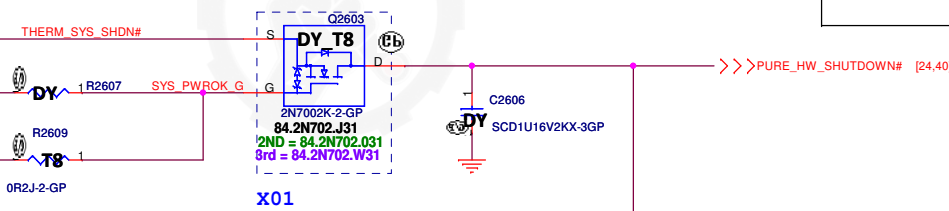
TEMPERATURE (°C)	T_CRIT#				
	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107
	7.5KΩ	79	89	99	109
	10.5KΩ	81	91	101	111
	14KΩ	83	93	103	113
	18.7KΩ	85	95	105	115



pull-high at p.24  
(3D3V\_S5)

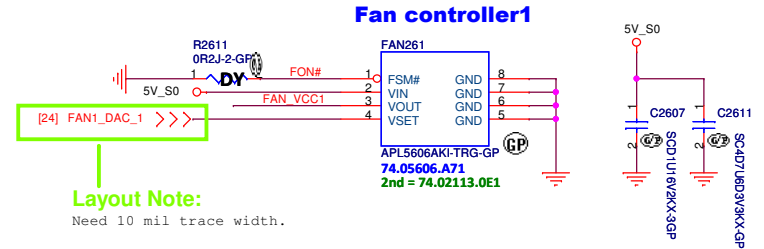


Thermal sensor NCT 7718W

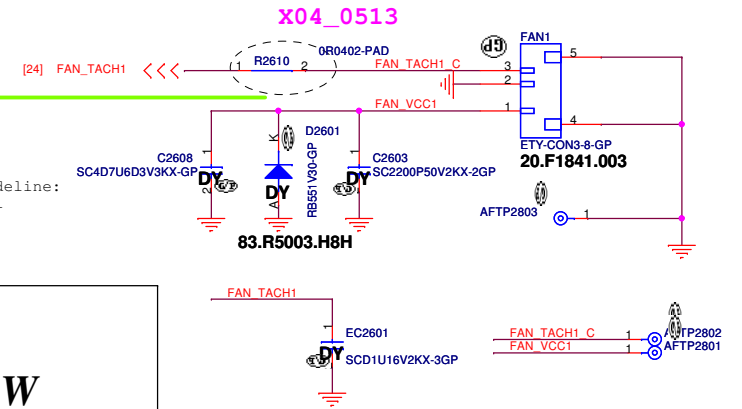


EE Note:  
R2608 need to fine tune base on thermal test.

Close to KBC  
VD\_IN1 for system thermal sensor



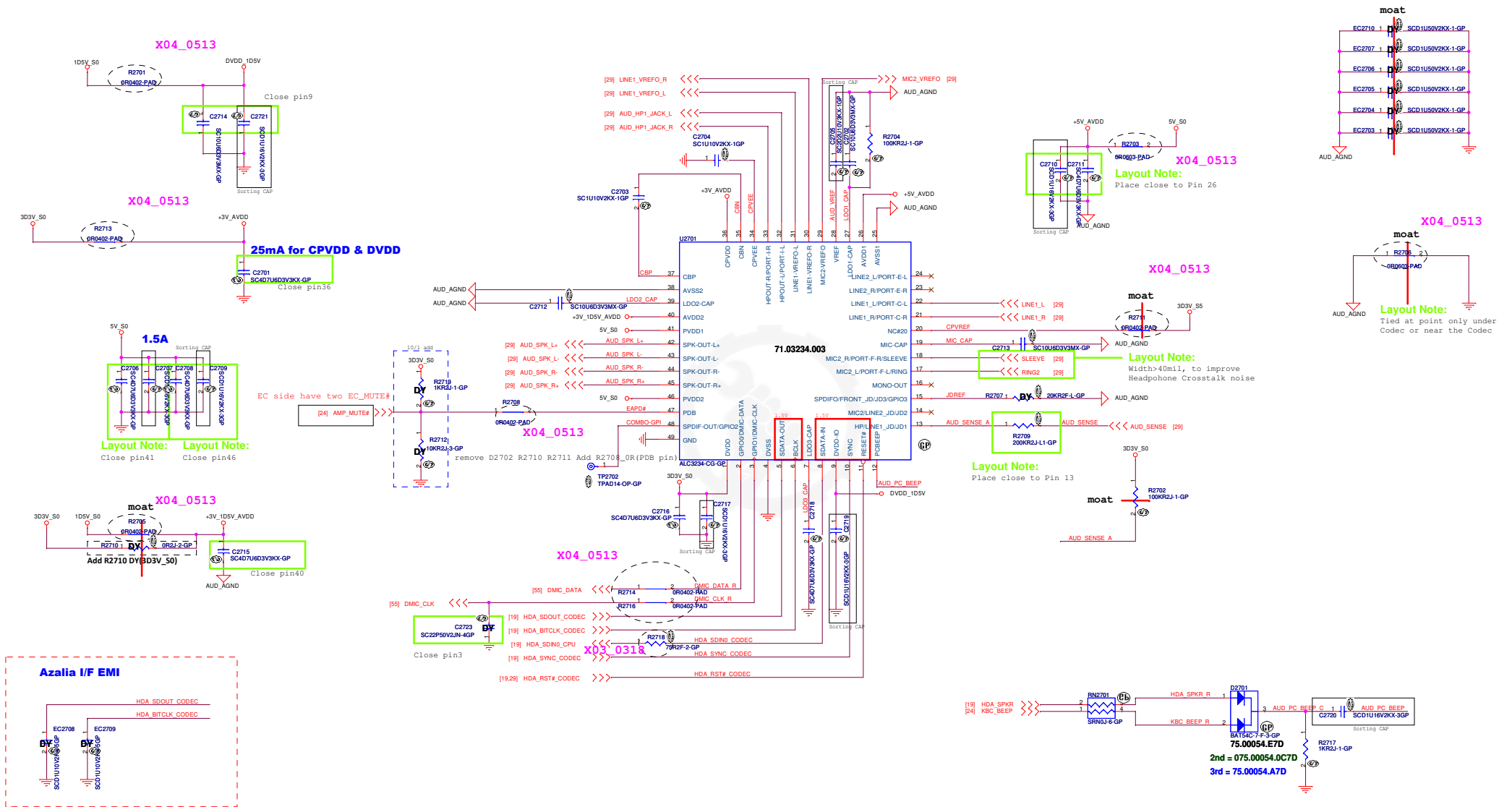
Layout Note:  
Need 10 mil trace width.



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Title: Thermal/Fan control  
Size: A3 Document Number: Iris BSW Rev: A00  
Date: Thursday, May 28, 2015 Sheet: 26 of 109



# Blanking

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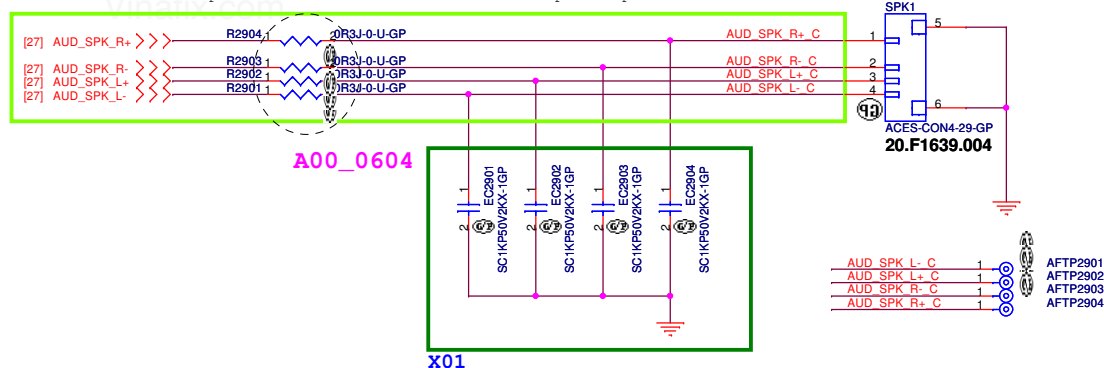
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)</b>			
Size A4	Document Number <b>Iris BSW</b>		Rev <b>A00</b>
Date: Thursday, May 28, 2015		Sheet 28 of	109

Main Func = Audio

# Speaker

## Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power

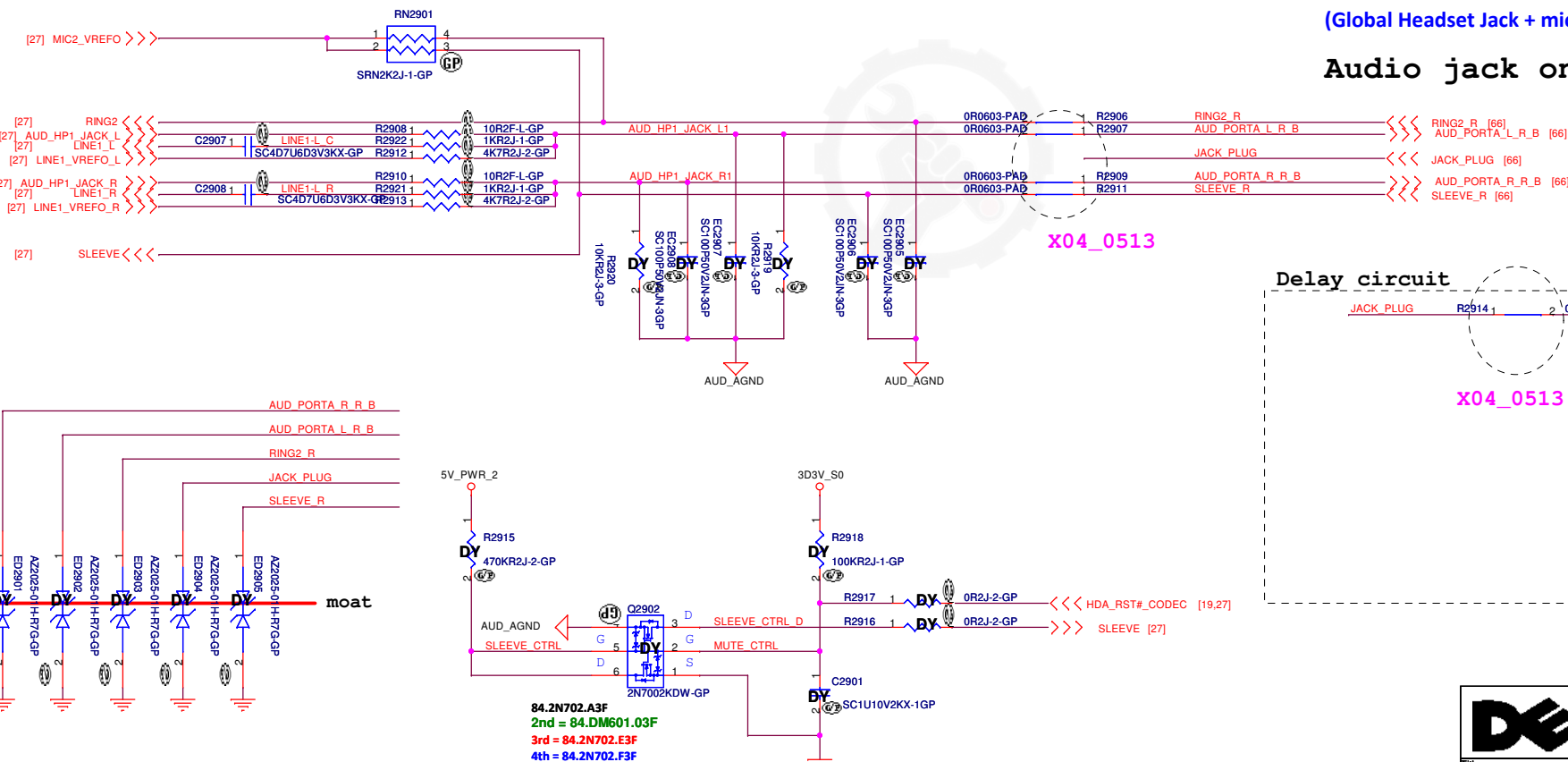


Main Func = Audio

## Universal Jack

(Global Headset Jack + mic phone in + line in support)

Audio jack on I/O Board.



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Title		MIC/SPEAKER/AUDIOJACK	
Size	Custom	Document Number	Rev
Date: Thursday, June 04, 2015		Iris BSW A00	
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Main Func = LAN

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Title <b>(Reserved)</b>			
Size A4	Document Number <b>Iris BSW</b>		Rev <b>A00</b>
Date: Thursday, May 28, 2015		Sheet 30 of	109


Main Func = LAN

Vinafix.com

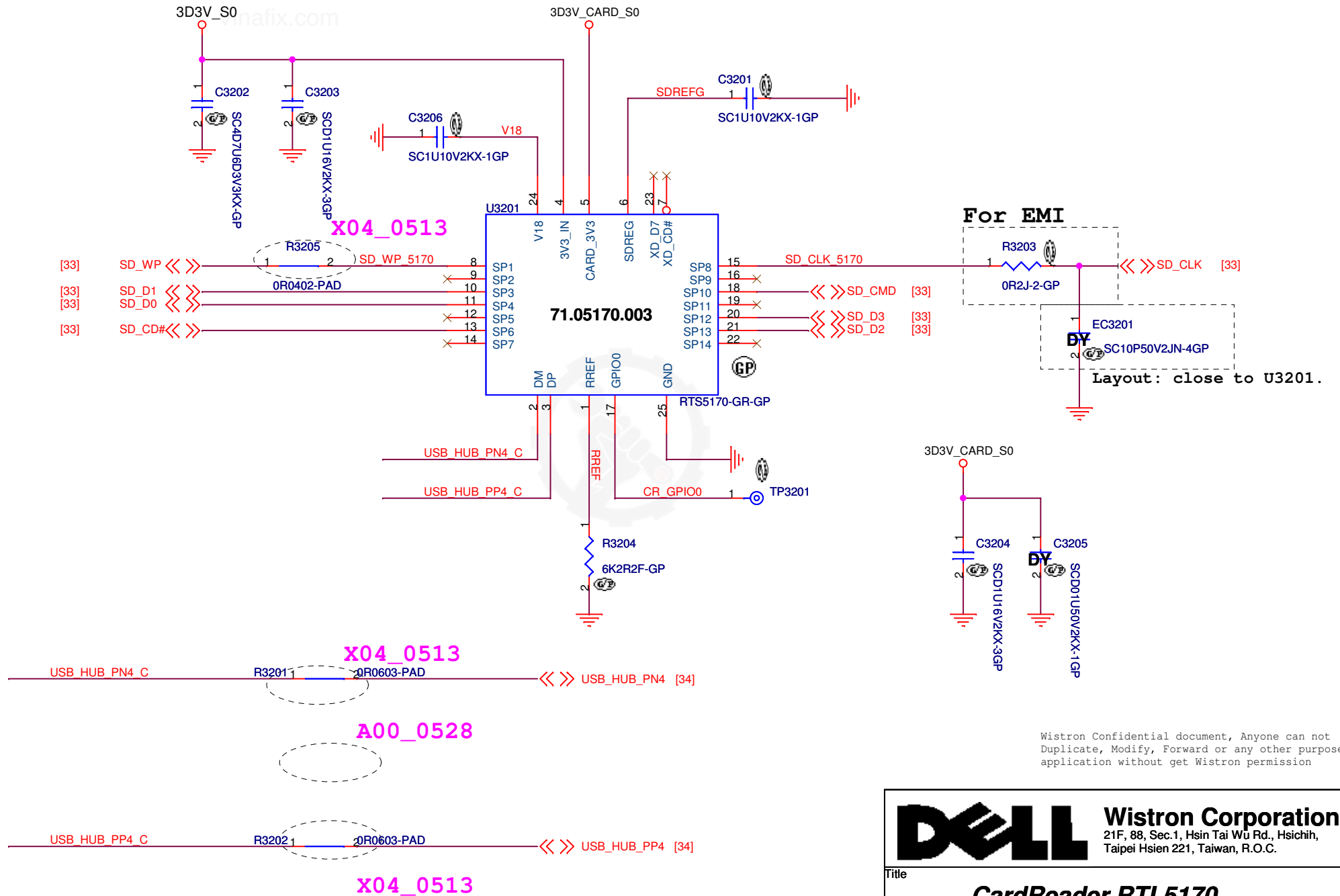
# Blanking



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Title <b>(Reserved)</b>			
Size A4	Document Number <b>Iris BSW</b>		Rev <b>A00</b>
Date: Thursday, May 28, 2015		Sheet 31 of	109

# Main Func = Card Reader



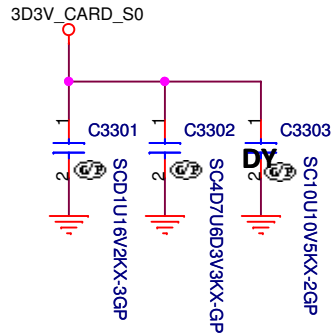
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>CardReader RTL5170</b>			
Size	Document Number		Rev
A4	<b>Iris BSW</b>		<b>A00</b>
Date:	Thursday, May 28, 2015		Sheet 32 of 109

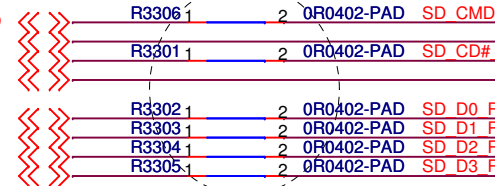


# Main Func = Card Reader

Vinafix.com



[32] SD\_CMD  
[32] SD\_CLK  
[32] SD\_CD#  
[32] SD\_WP  
[32] SD\_D0  
[32] SD\_D1  
[32] SD\_D2  
[32] SD\_D3

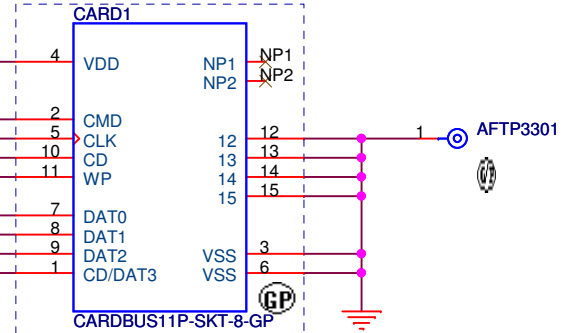


X04\_0513

3D3V\_CARD\_S0

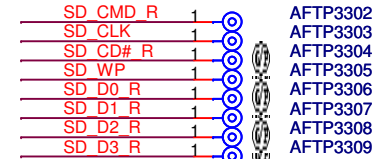
400mA

X01

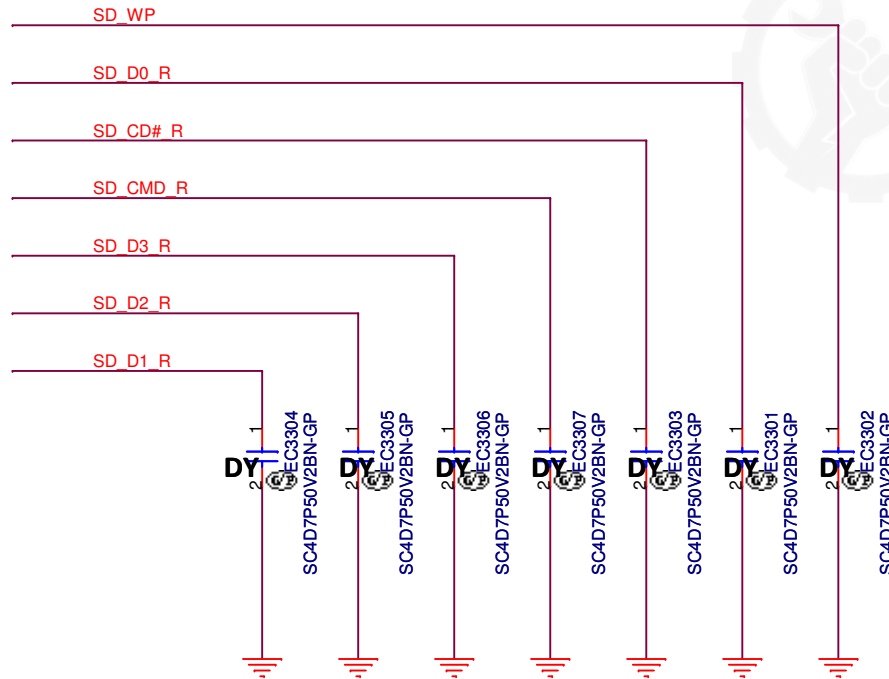


MAIN = 020.I0002.0001

2ND = 062.I0002.0251



For EMI Reserved



Without card	
Inserted card(lock)	
Inserted card(unlock)	

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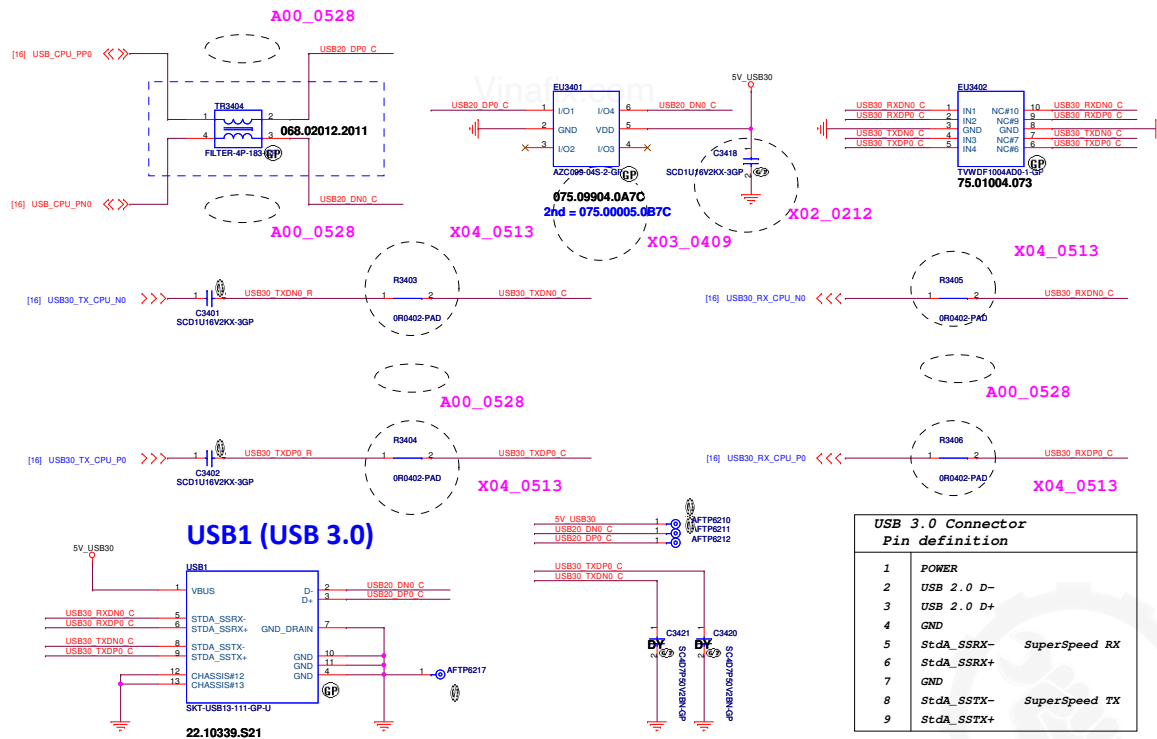
Title

**Card Reader CONN**

Size A4 Document Number **Iris BSW** Rev **A00**

Date: Monday, June 01, 2015 Sheet 33 of 109

## Main Func = USB3.0 Port1



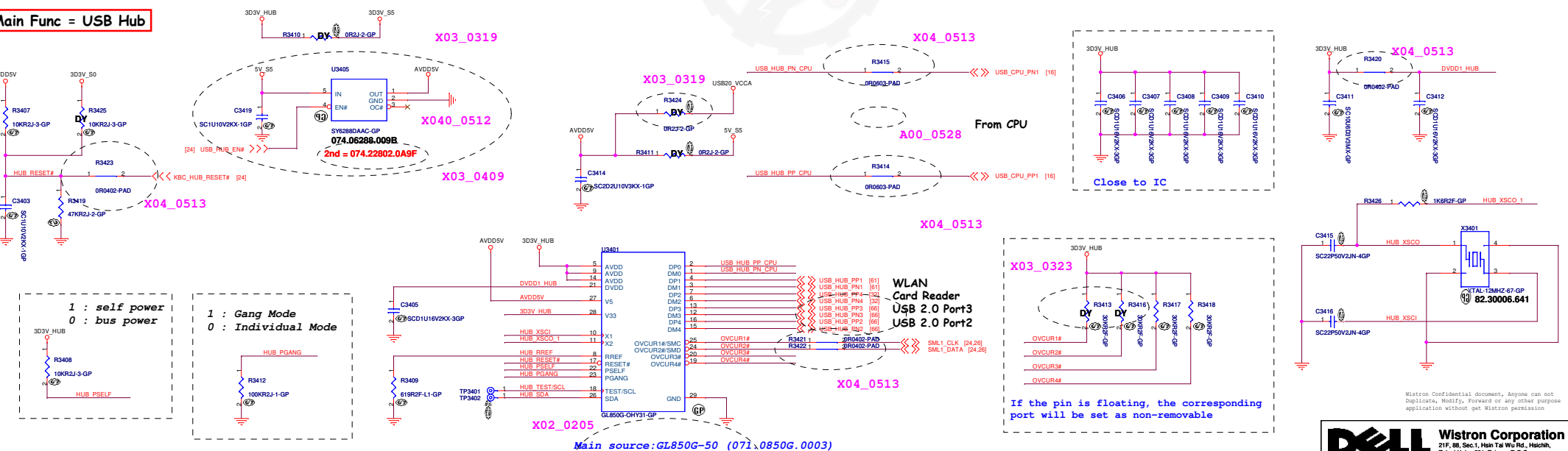
## Main Func = USB2.0 Port2

USB connector on I/O Board.

## Main Func = USB2.0 Port3

USB connector on I/O Board.

## Main Func = USB Hub



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File  
**USB2.0/3.0 CONN/USB Hub**  
Size  
A2  
Document Number  
**Iris BSW**  
Date  
Friday, June 05, 2015  
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34  
of  
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Rev  
**A00**

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Title

***USB3.0 CONN (Reserved)***

Size

Document Number

Rev

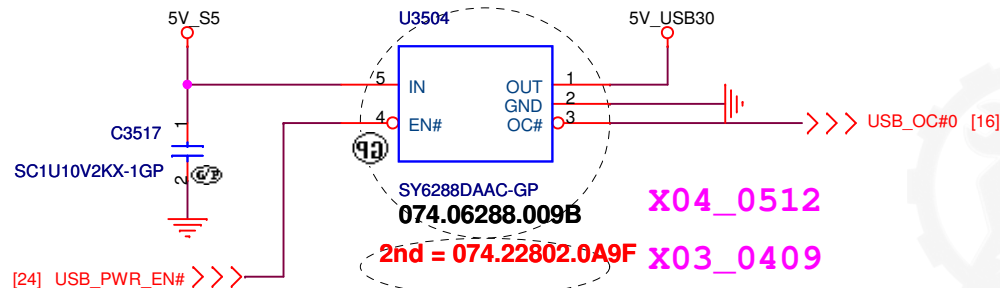
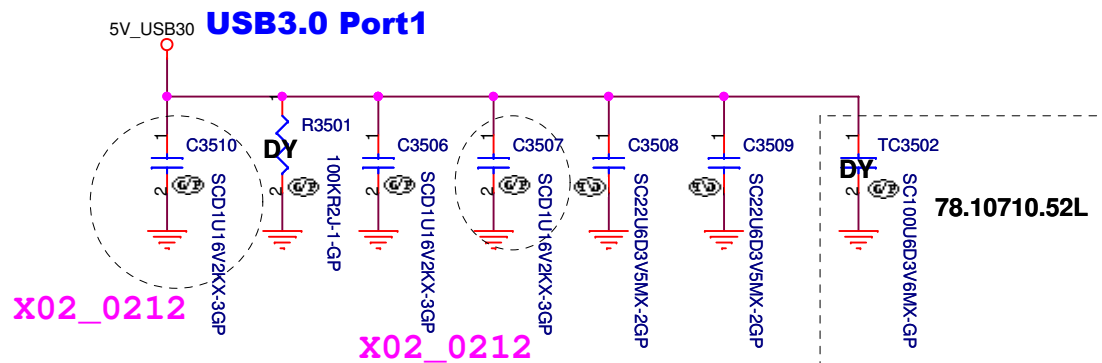
***Iris BSW***

***A00***

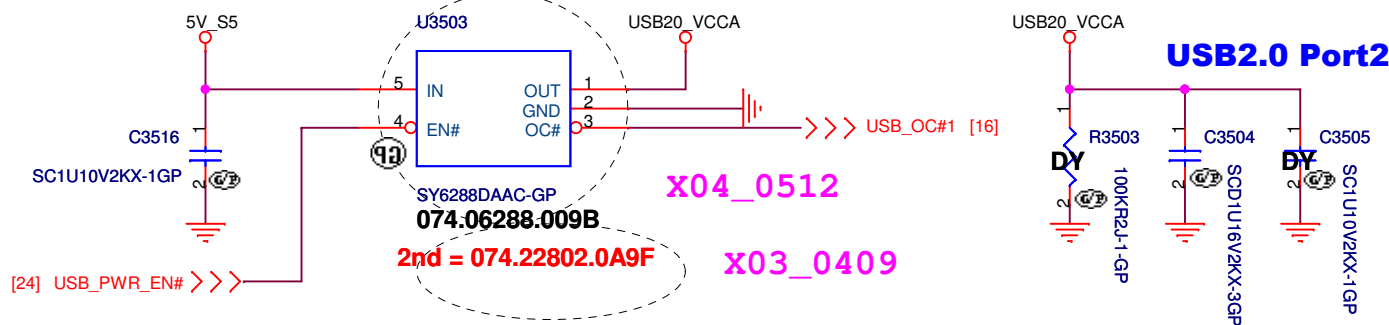
Date: Thursday, May 28, 2015

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## Main Func = USB3.0



## Main Func = USB2.0



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Title			
<b>USB2.0 HUB(Reserved)</b>			
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	<b>Iris BSW</b>		<b>A00</b>
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Title

*(Reserved)*

Size  
A4

Document Number  
**Iris BSW**


Rev  
**A00**

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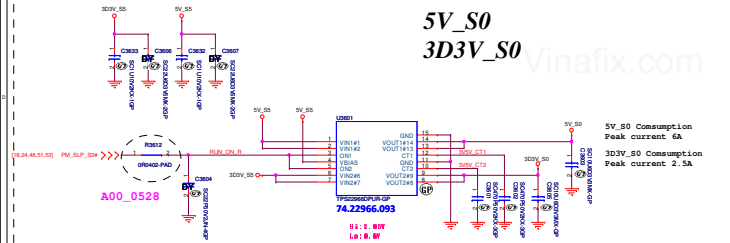
# Blanking

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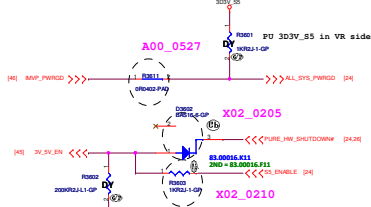
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)</b>			
Size A4	Document Number <b>Iris BSW</b>		Rev <b>A00</b>
Date: Thursday, May 28, 2015		Sheet 39 of	109

# Main Func = Power Plane & Sequence

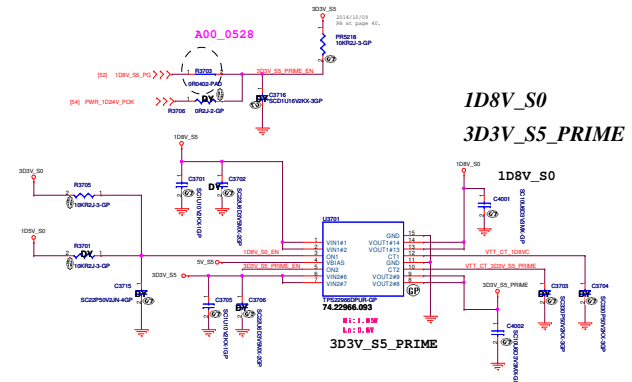
## 5V\_S0 3D3V\_S0



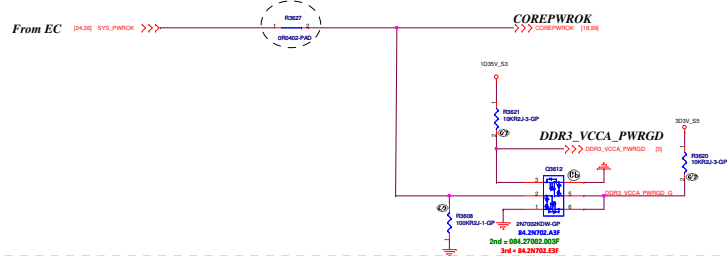
## Power Good



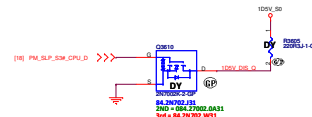
## 1D8V\_S0 3D3V\_S5\_PRIME



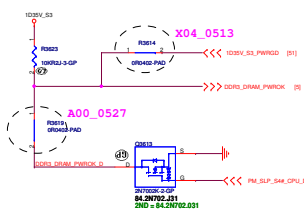
## DDR3\_VCCA\_PWRGD



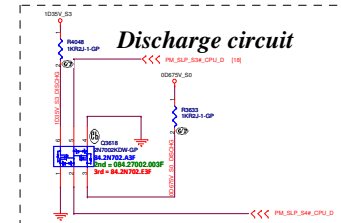
## Discharge circuit



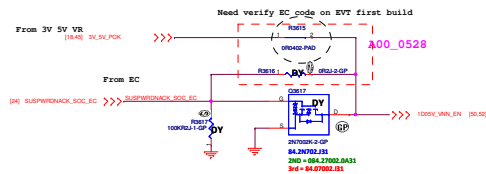
## DDR3\_DRAM\_PWROK



## Discharge circuit




Need verify EC code on EVT first build





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Size A4	Document Number <b>Iris BSW</b>		Rev <b>A00</b>
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Title

**(Reserved)**

Size  
A

Document Number

**Iris BSW**

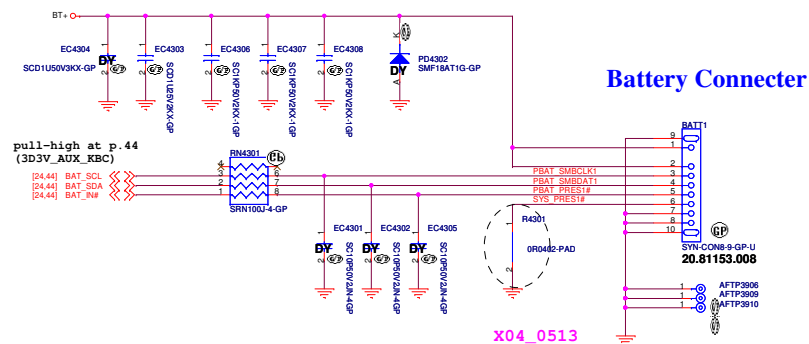
Rev

**A00**

Date: Thursday, May 28, 2015

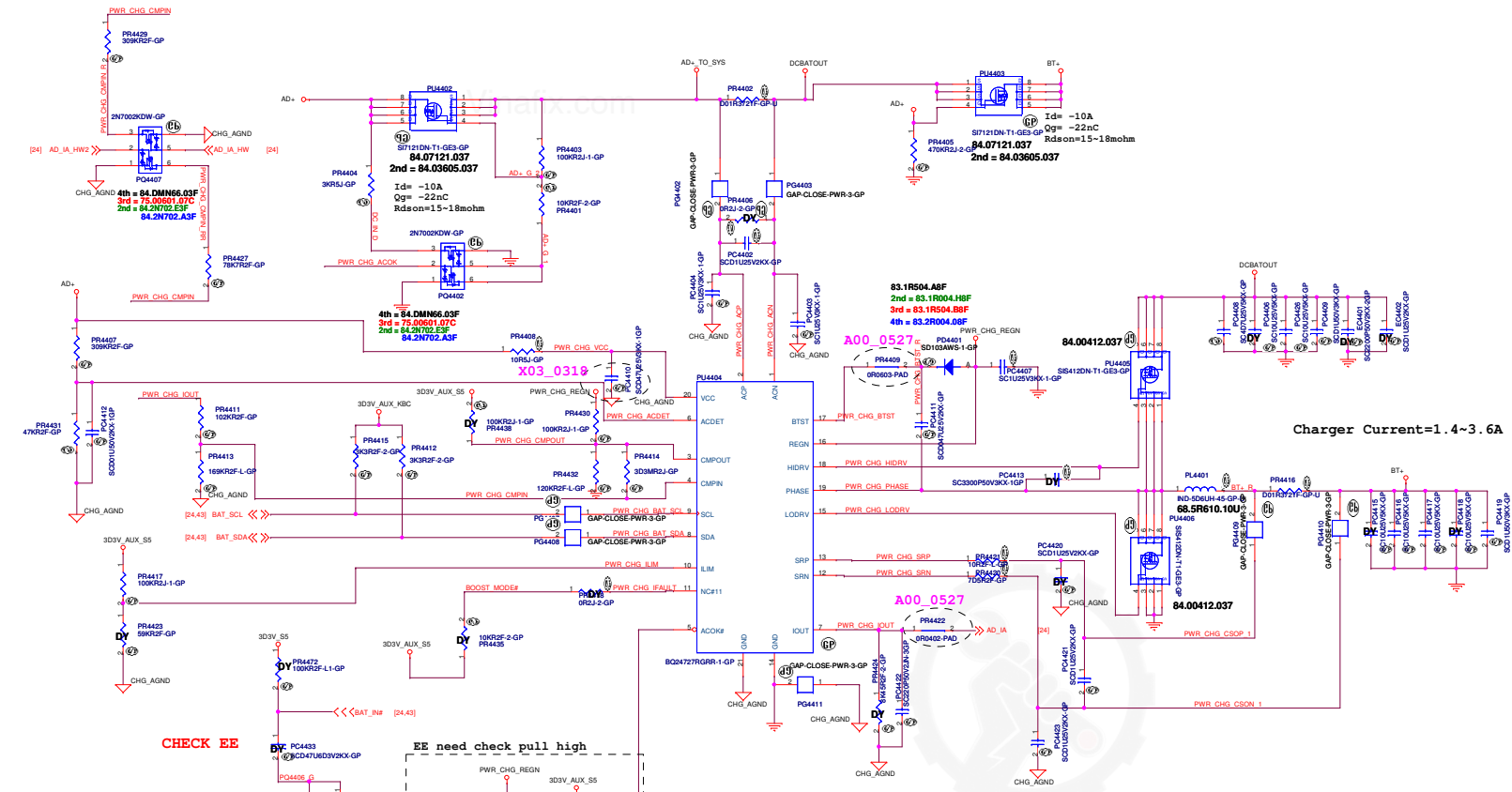
Sheet 42 of 109

**Placement:** Close to Batt Connector

[illegible]

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# Main Func = Charger



CHECK EE

EE need check pull high

AC\_IN#

H\_PROCHOT#

84.2N702.J31

84.2N702.E11

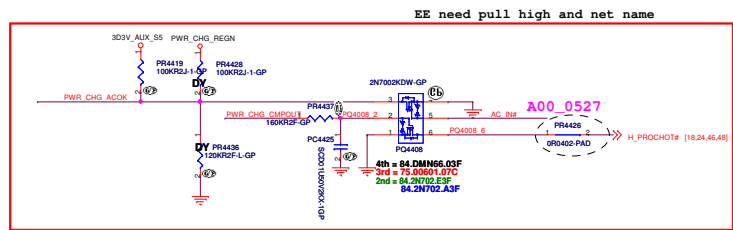
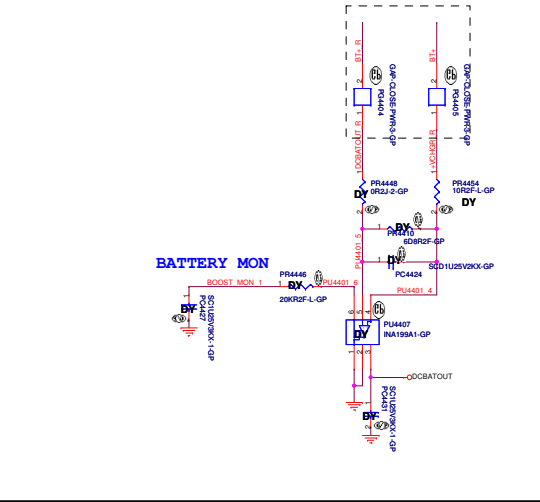
84.2N702.E3F

84.2N702.E3F

84.2N702.E3F

84.2N702.E3F

## Customer Request

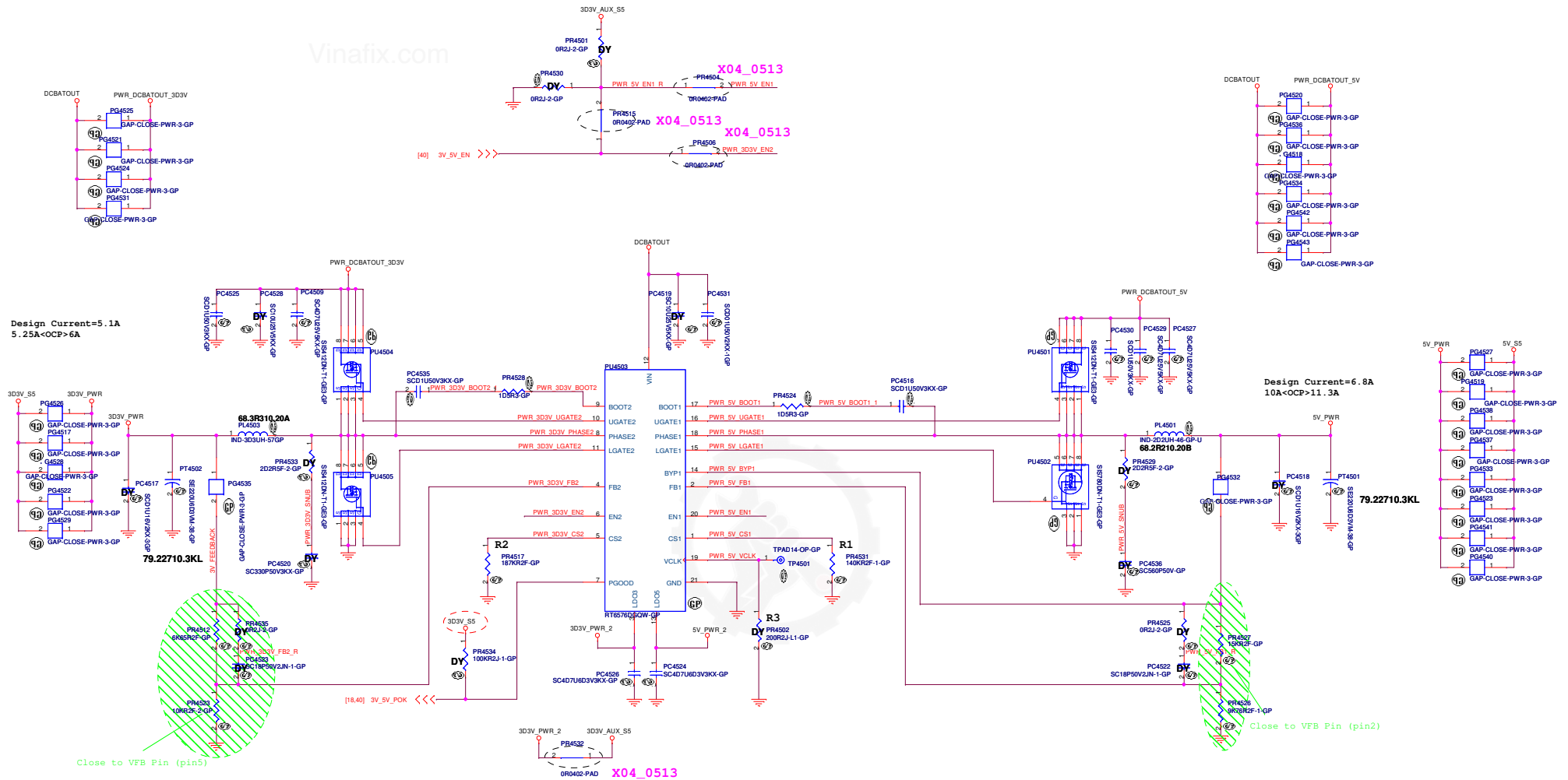


EC code only BQ24727

H_PROCHOT#	AD_IA_HW	AD_IA_HW2
35W	0	0
45W	1	0
65W	0	1

Main Func = 3D3V\_5V

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I/P cap: CHIP CAP C 10U 25V X8085 X5R/ 78.10622.51L  
Inductor: CHIP INO 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A  
O/P cap: CHIP CAP EL 220U 6.3V M6.3+4.4 /Chemt-con / 18mOhm / 79.22710.3KL  
H/S: SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037  
L/S: SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037

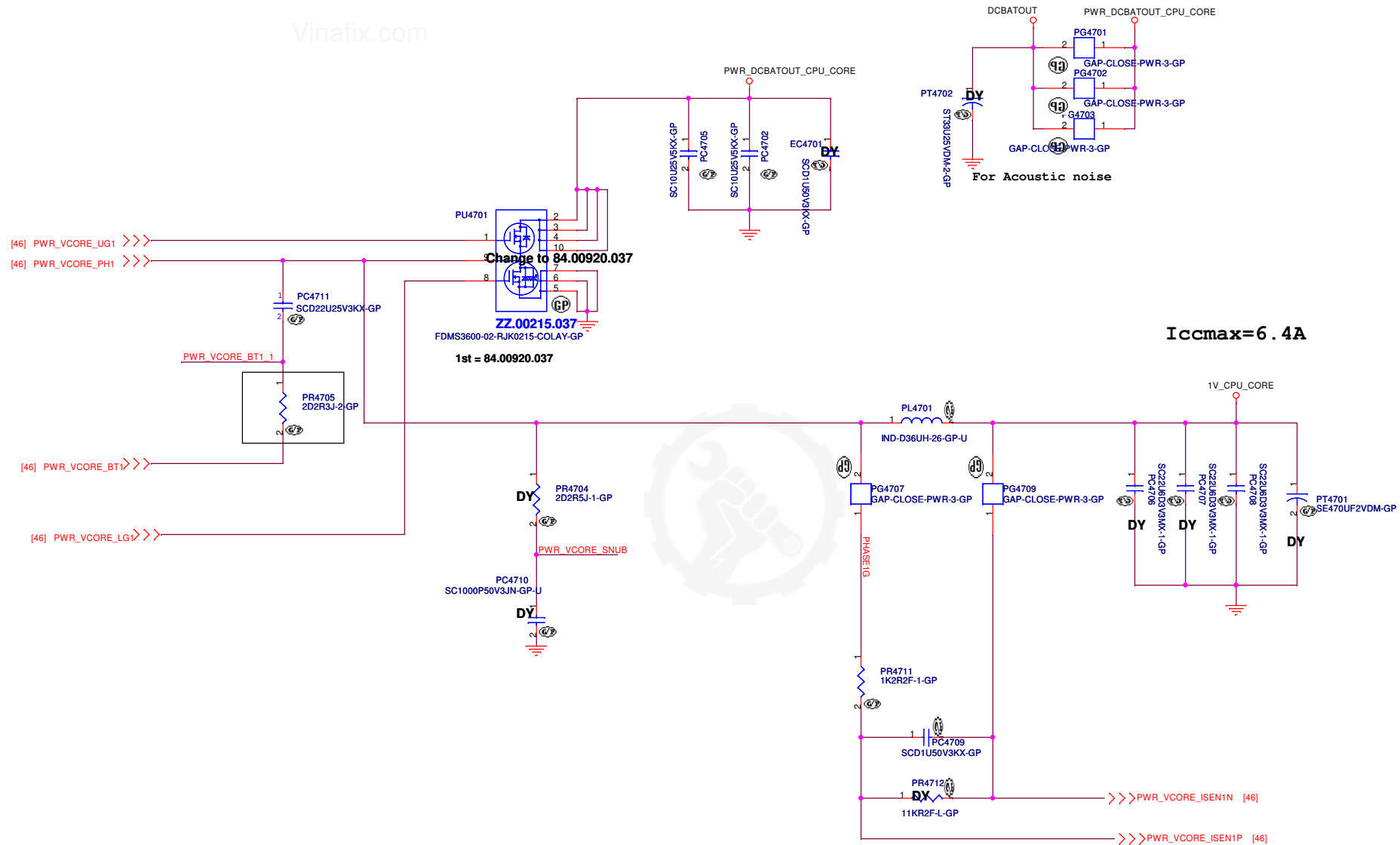
I/P cap: CHIP CAP C 10U 25V X8085 X5R/ 78.10622.51L  
Inductor: CHIP CHOK 2.2U PCMC063T-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B  
O/P cap: CHIP CAP EL 220U 6.3V M6.3+4.4 /Chemt-con / 18mOhm / 79.22710.3KL  
H/S: SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037  
L/S: SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

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# SSID = CPU Regulator

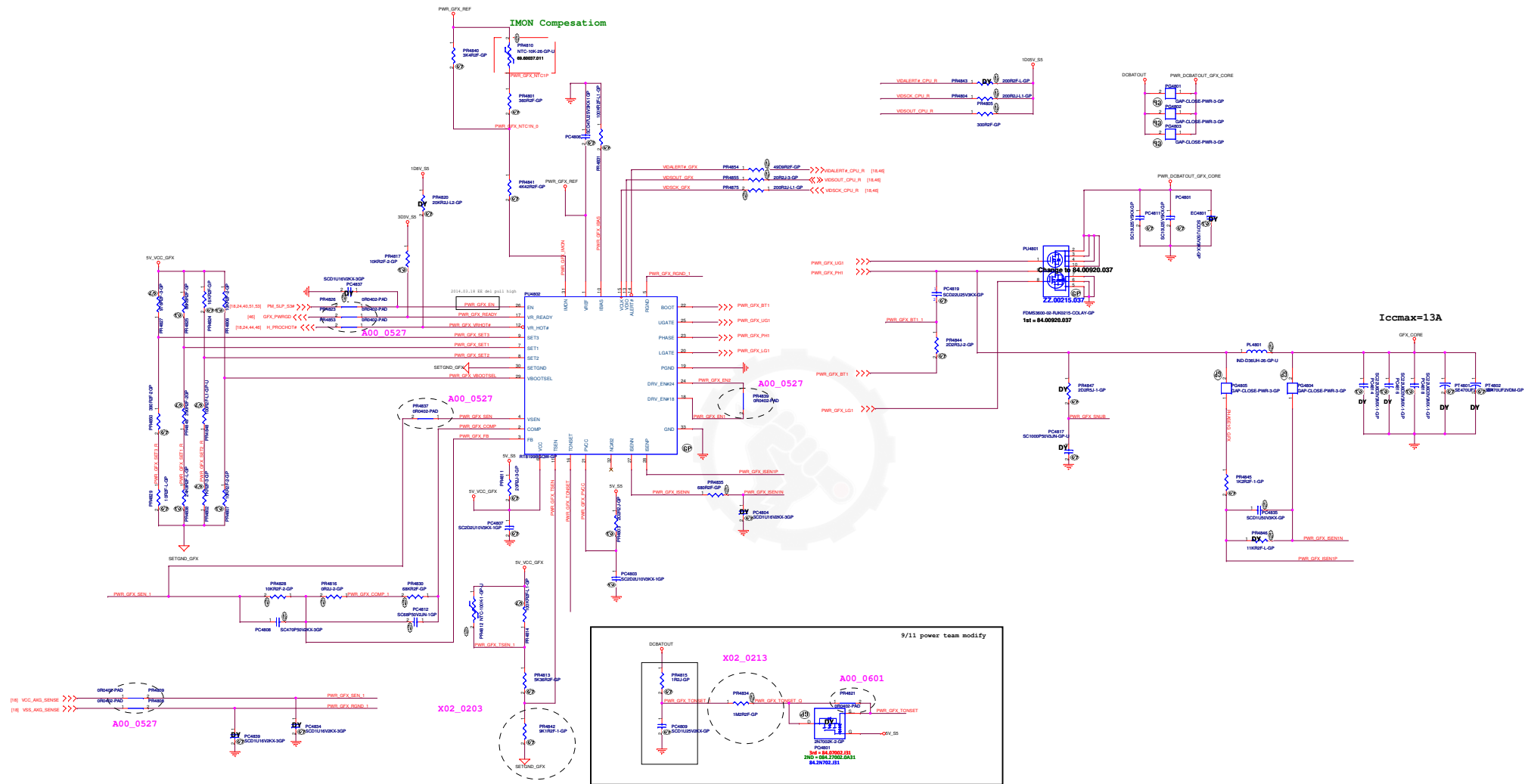
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Iccmax=6.4A

<Core Design>

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Title

***PWR Plane Enable & Sequence***

Size  
A4

Document Number

**Iris BSW**

Rev  
**A00**

Date: Thursday, May 28, 2015

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***SY8206D for 1D05V*** x04\_0513



## SYW232 for 1D15V\_S5

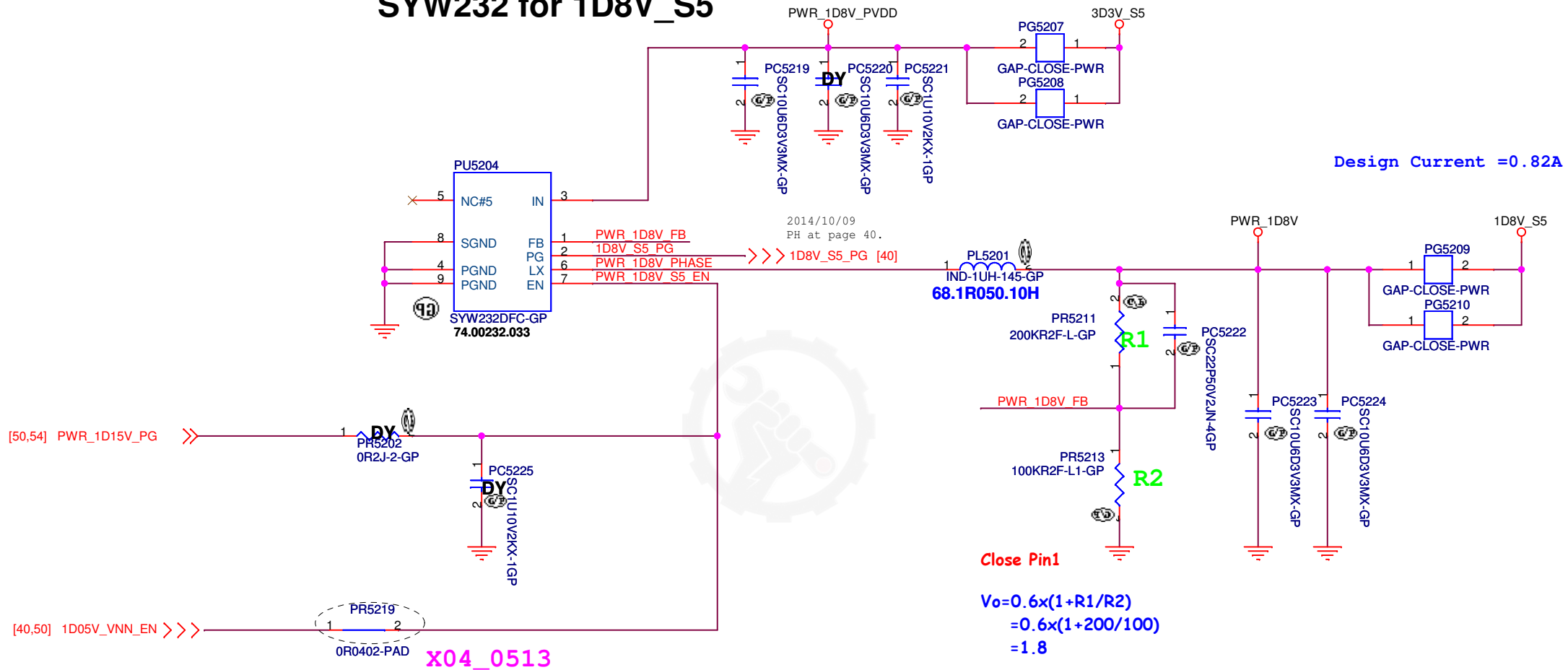




SSID = PWR.Plane.Regulator\_1p8v

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## SYW232 for 1D8V\_S5



<Core Design>



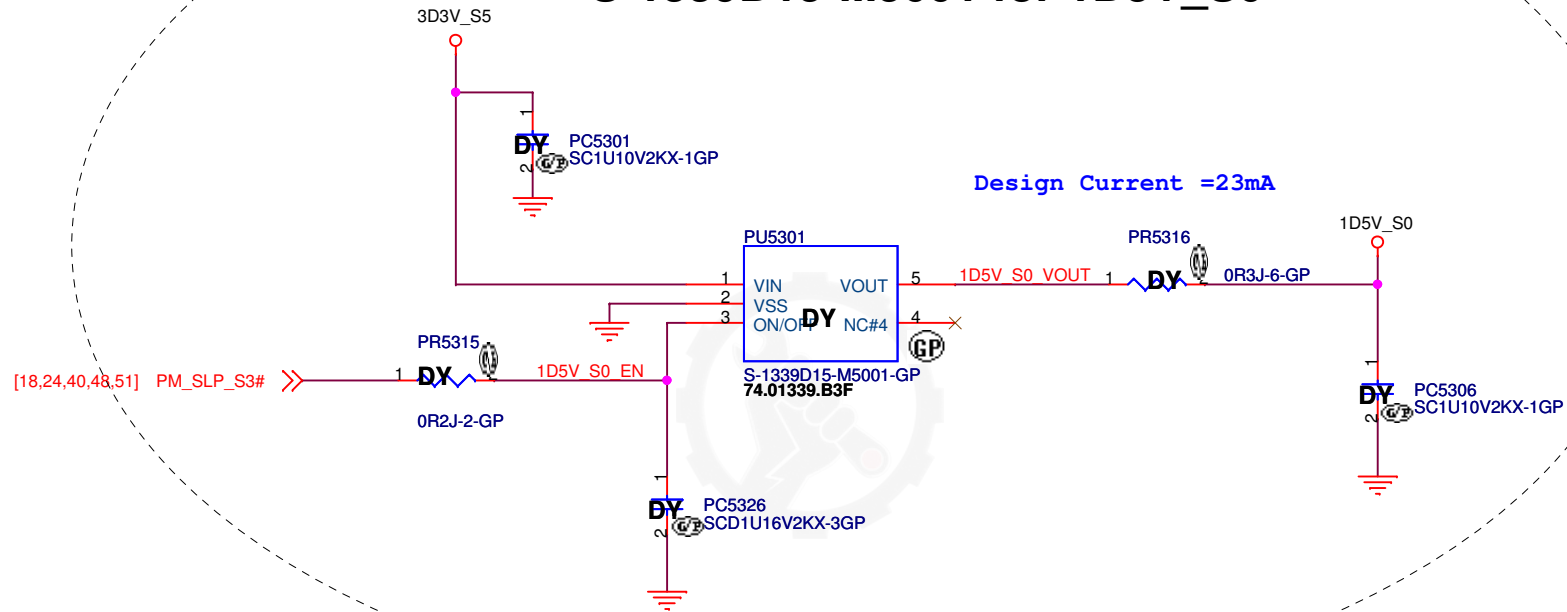
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Title			SYW232DFC_1D8V
Size	Document Number	Rev	A00
A4			
Date:	Thursday, May 28, 2015	Sheet	52 of 109

x02\_0212

**S-1339D15-M5001 for 1D5V\_S0**



## <Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title
-------

**S1339D15 1D5V**

Size  
A4

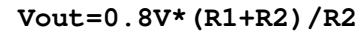
Document Number
-----------------

Rev  
**A00**

Date: Thursday, May 28, 2015

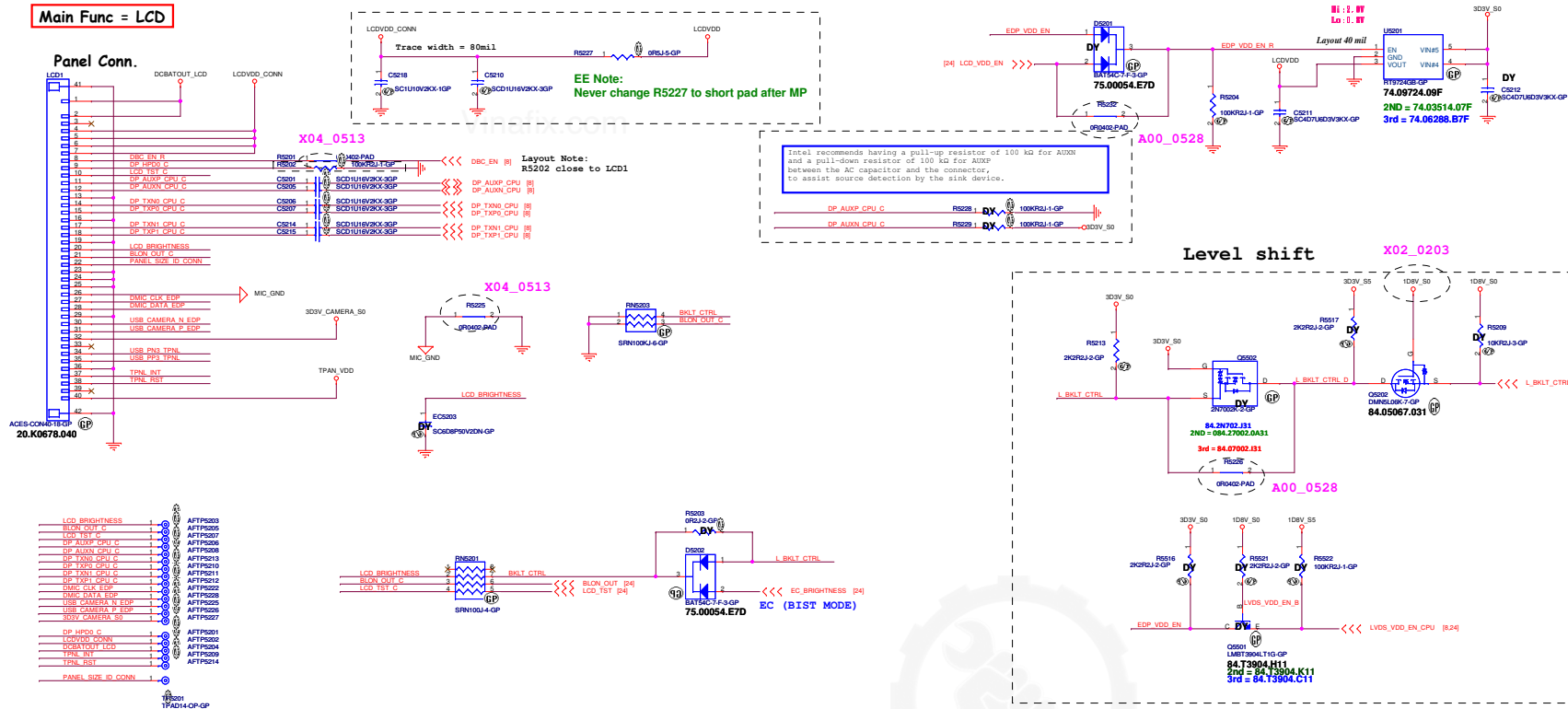
Sheet 53 of 109

X03\_0319  
X03\_0310  
A00\_0528



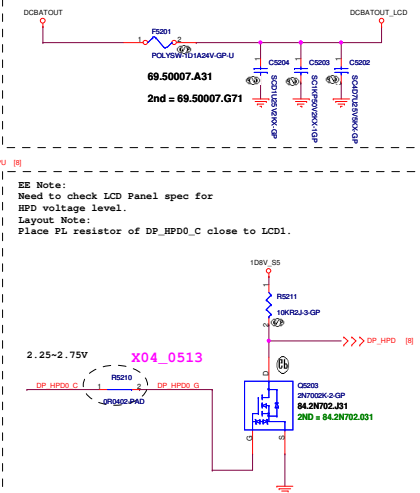
Title			
APL5930_1D24V			
Size A3	Document Number		Rev A00
Date: Thursday, May 28, 2015	Sheet	54 of	109

**Main Func = LCD**



### INVERTER POWER

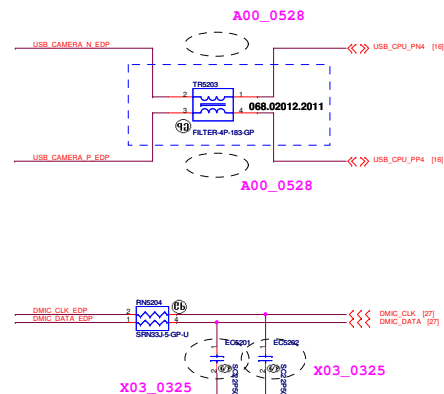
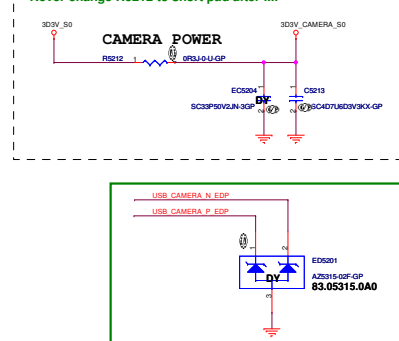
**EE Note:**  
**Never change R5208 to short pad after MP**



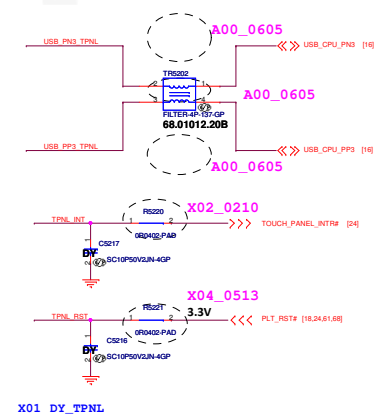
**Main Func = Camera + DMIC**

## Camera + Microphone

**EE Note:**  
Never change R5212 to short pad after MP

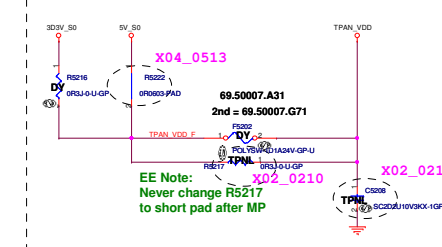


**Main Func = TS**




## Touch Screen

TOUCH PANEL POWER



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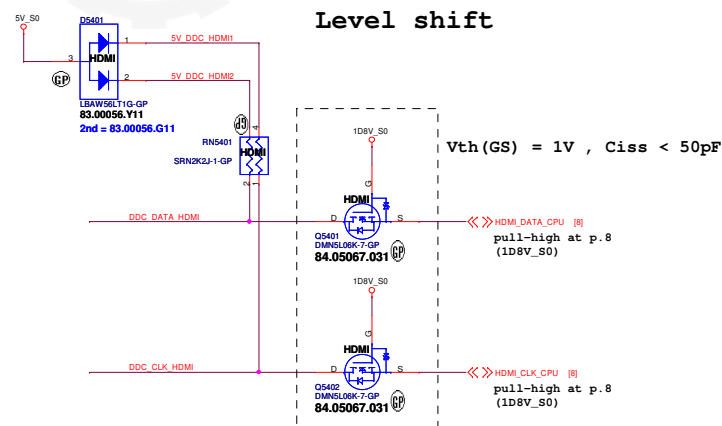
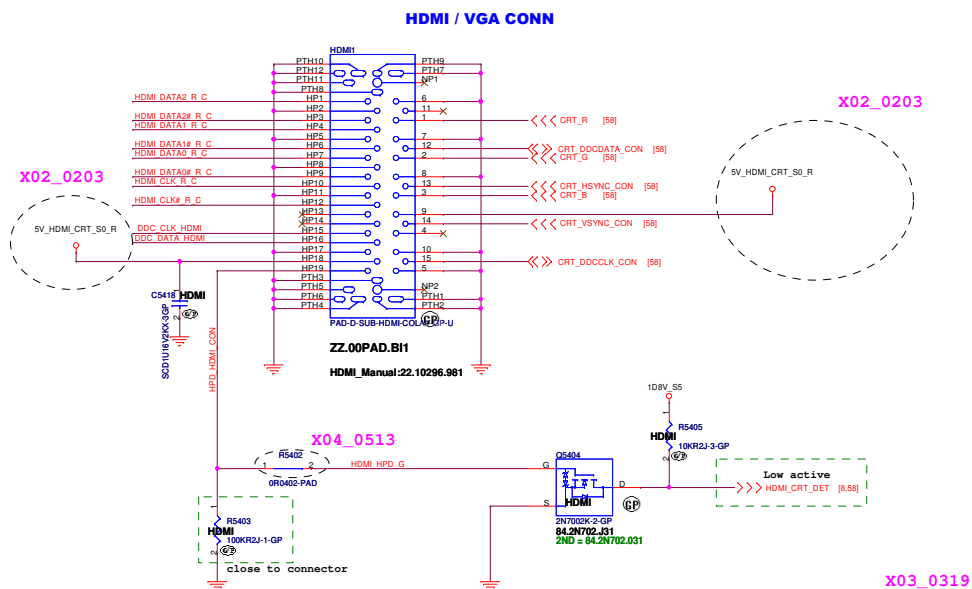
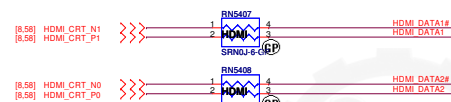
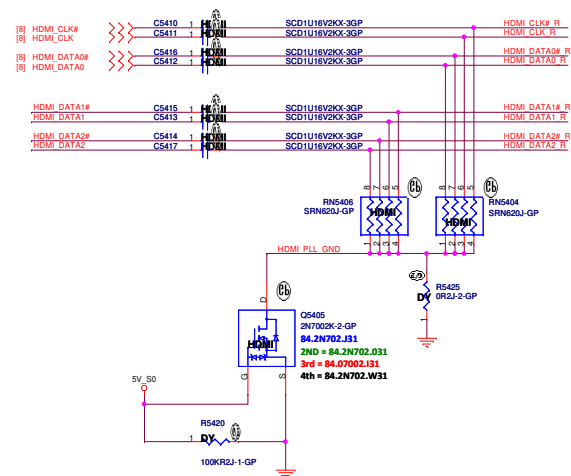
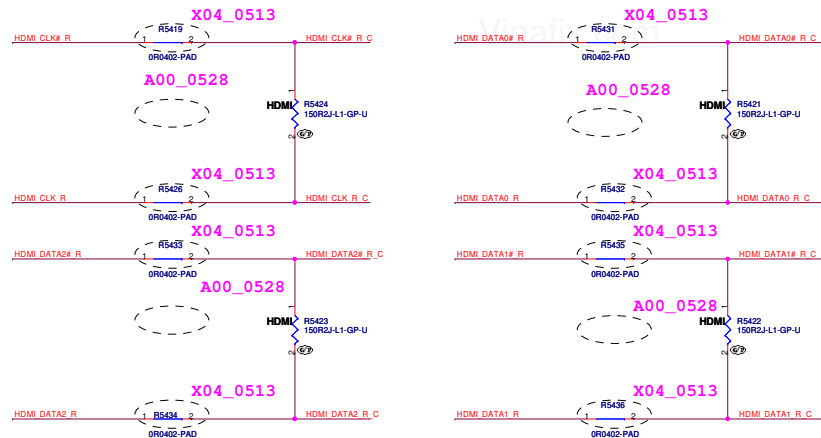
# Blanking

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<b><i>Reserved</i></b>			
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Main Func = HDMI

## HDMI Level Shifter & Connector

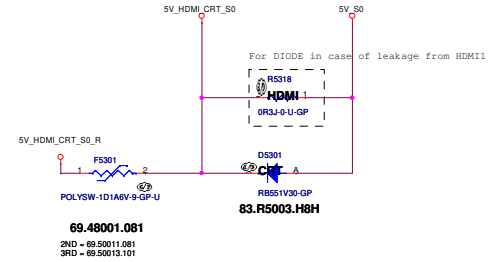


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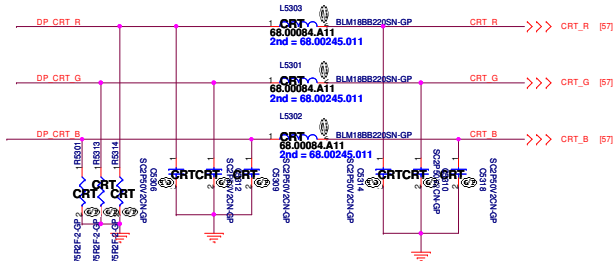
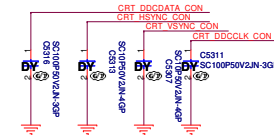
		POL1_SDA(PIN22)		ng device
		0	1	
POL2_SCL(PIN23)	0	X		EP MODE
	1	ROM ONLY MODE		EEPROM MODE

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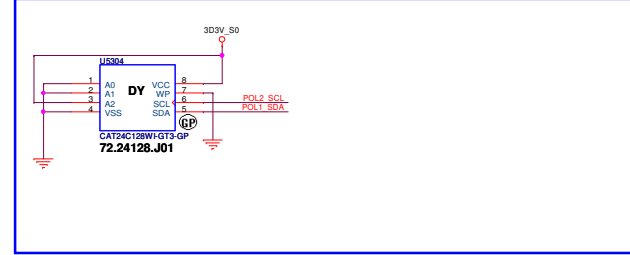
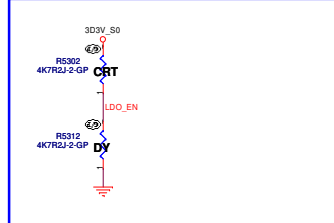
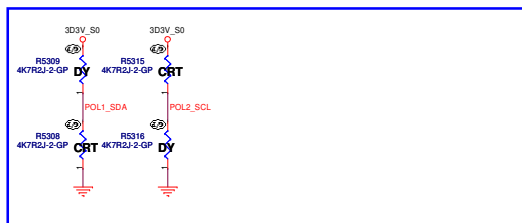
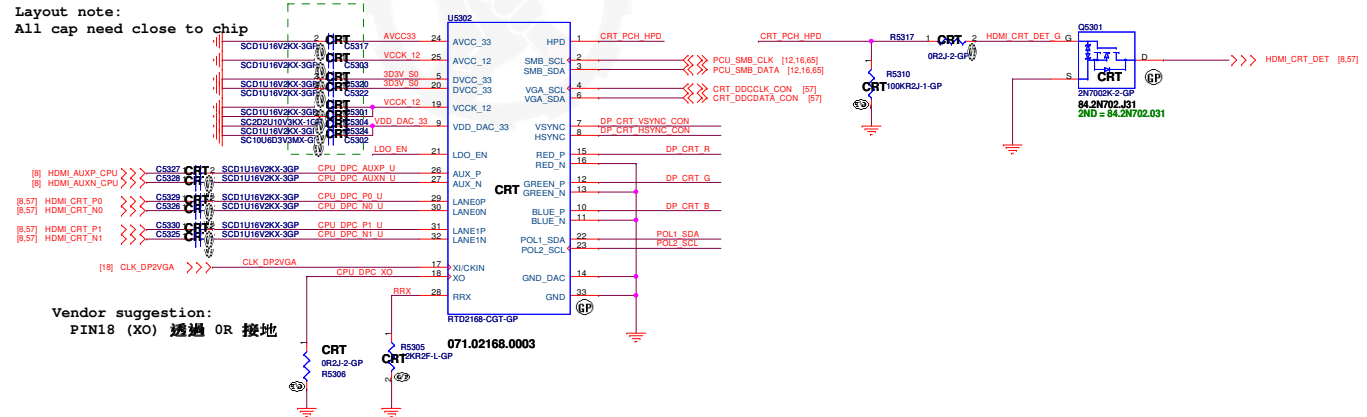
CRT\_R 1 AFTP501 AFTE14P-GP  
 CRT\_G 2 AFTP502 AFTE14P-GP  
 CRT\_B 3 AFTP503 AFTE14P-GP  
 5V HDMI CRT\_S0\_R 4 AFTP504 AFTE14P-GP  
 CRT\_DDDATA\_CON 5 AFTP505 AFTE14P-GP  
 CRT\_VSYNC\_CON 6 AFTP506 AFTE14P-GP  
 CRT\_HSYNC\_CON 7 AFTP507 AFTE14P-GP  
 AFTP508 AFTE14P-GP



CRT RGB  
 CRT H/VSYNC  
 CRT SMBUS




Layout note:  
 All cap need close to chip



Main Func = WLAN

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Document Number  
**Iris BSW**

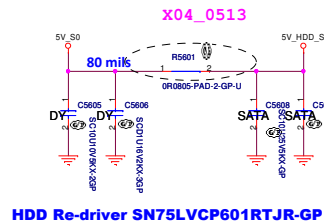
Rev  
**A00**

Date: Thursday, May 28, 2015

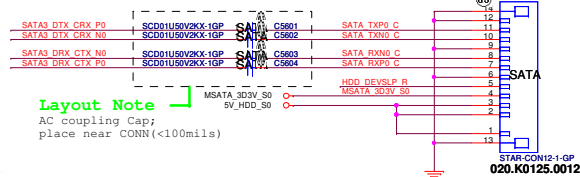
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Main Func = HDD

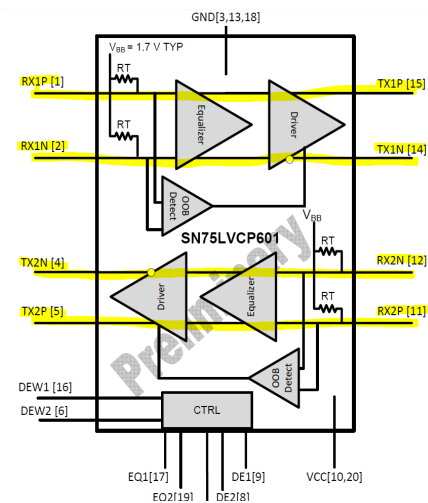
## SATA HDD Connector



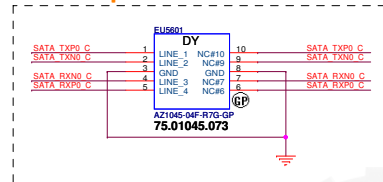
[19] HDD\_DEVSLP\_R >>> HDD\_DEVSLP\_R



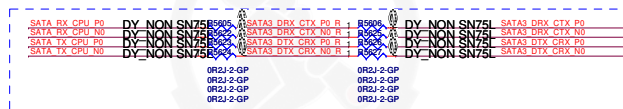
**HDD Re-driver SN75LVCP601RTJR-GP**



### EMI Request



**X01 NON HDD Re-driver**



**X01**

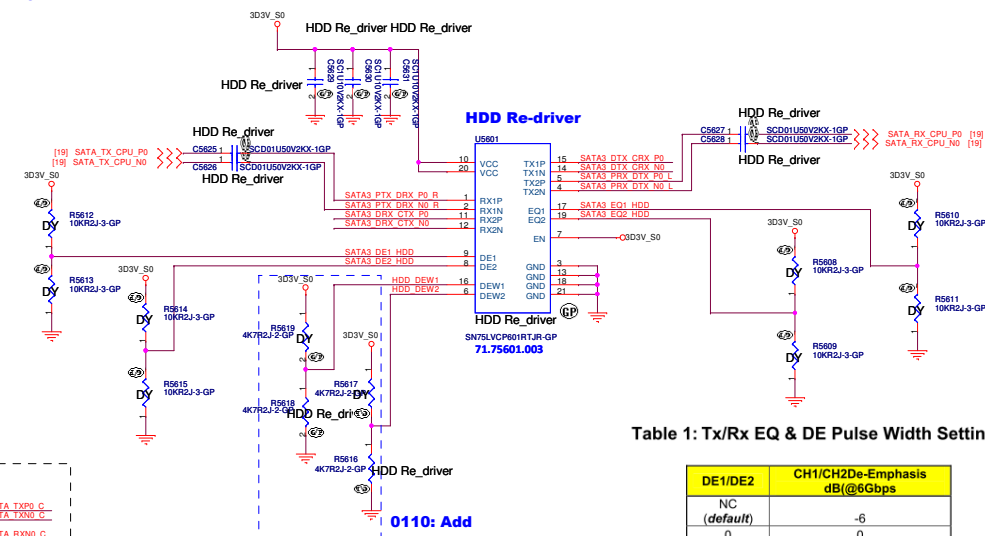


Table 1: Tx/Rx EQ & DE Pulse Width Settings

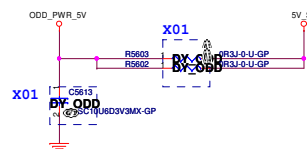
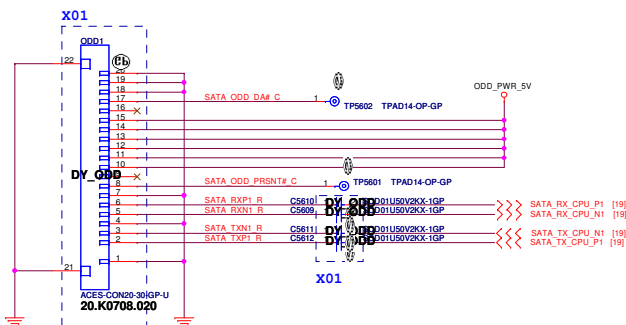
DE1/DE2	CH1/CH2De-Emphasis dB(@6Gbps)
NC (default)	-6
0	0
1	-3

EQ1/EQ2	CH1/CH2Equalization dB (@6Gbps)
NC (default)	0
0	7
1	14

DEW1/DEW2	Device Function→ DE Width for CH1/CH2
0	De-Emphasis Pulse Width Short (recommended setting when link operates at SATA 1.5/3.0/6.0 Gbps)
1 (default)	De-Emphasis Pulse Width Long (recommended setting when link operates at SATA 1.5/3.0 Gbps speed only)

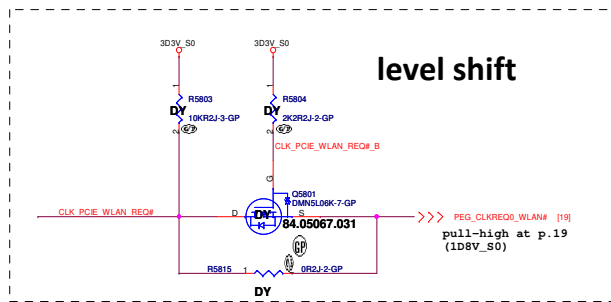
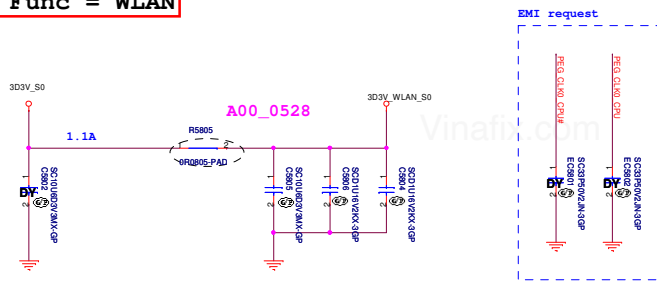
Main Func = ODD

## ODD Connector



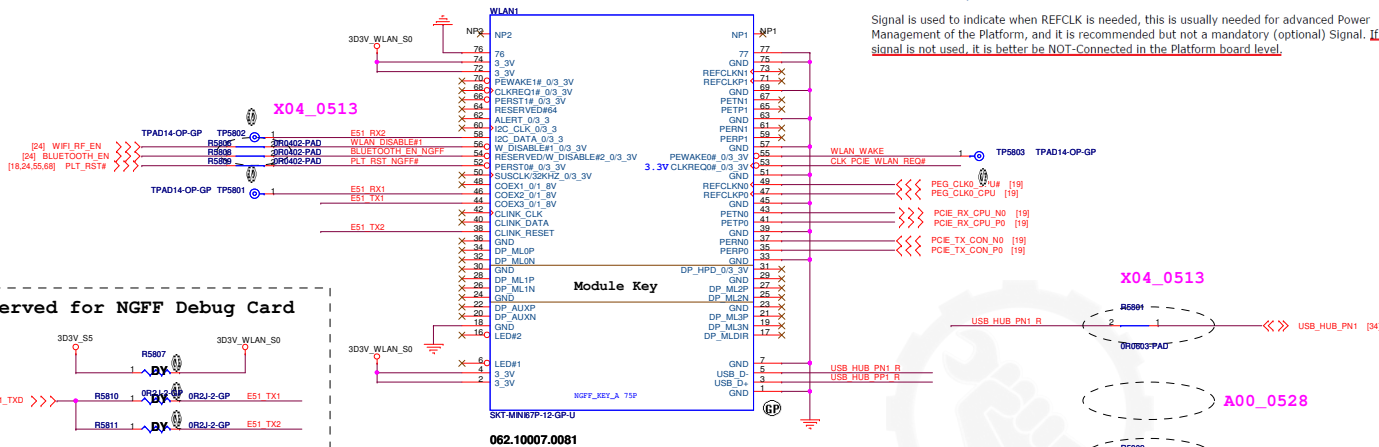
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**Main Func = WLAN**

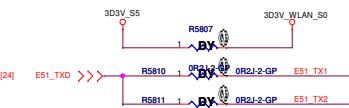


### 3.1.8.2 CLKREQ#

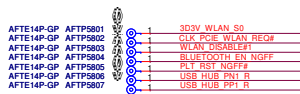
Signal is used to indicate when REFCLK is needed, this is usually needed for advanced Power Management of the Platform, and it is recommended but not a mandatory (optional) Signal. If the signal is not used, it is better be NOT-Connected in the Platform board level.



Reserved for NGFF Debug Card



EE Note:  
For NFGG Debug Card:  
Stuff R5807,R5810,R5811(optional).  
DY R5805.



SSID = WWAN


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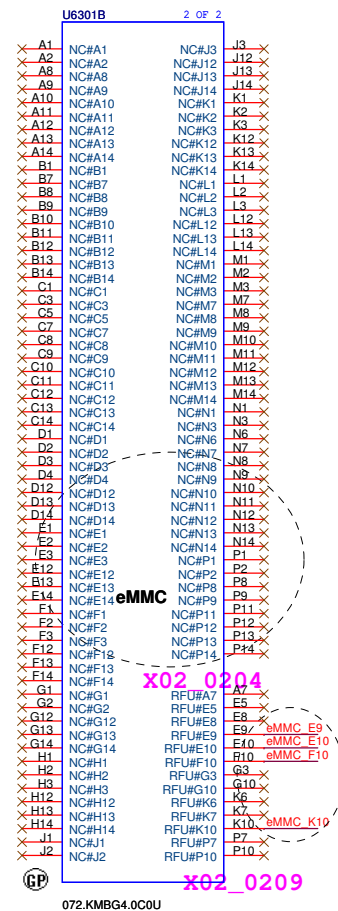
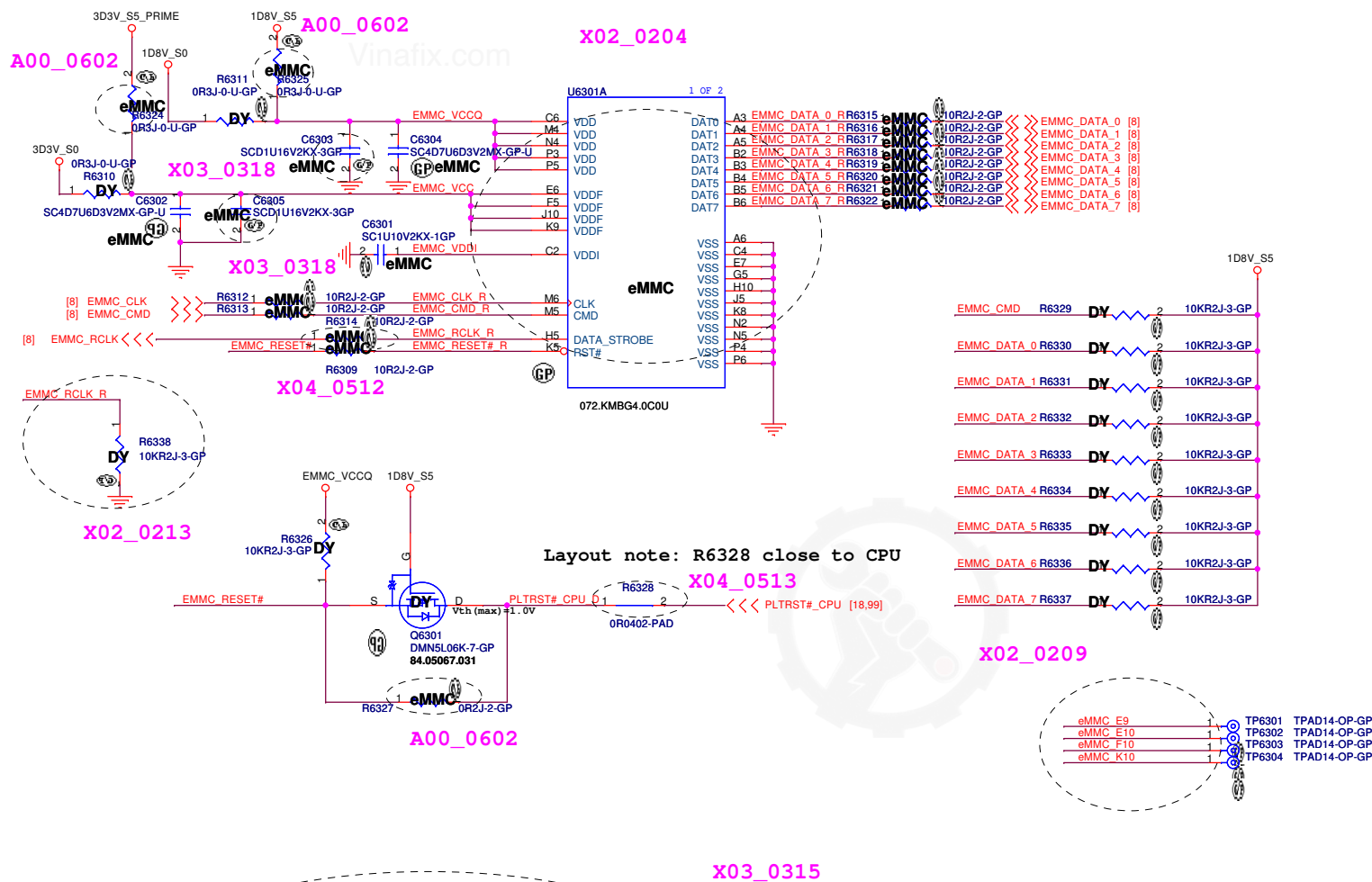


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<Core Design>

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**Main Func = mSATA**



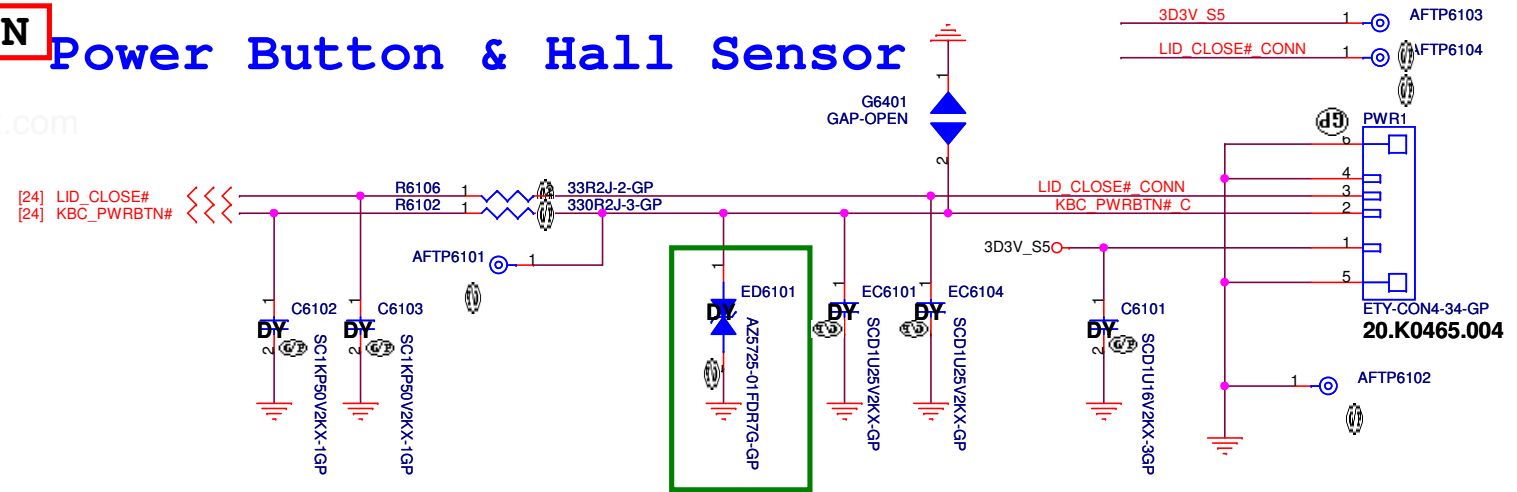
	SKU1		SKU1.1		SKU2		SKU3	
CPU	BRASWELL 2c FCBGA 1.6GHz 6W, GT 12EU, CELERON QS QJ4V	071.00BSW.0D0U	BRASWELL 2c FCBGA 1.6GHz 6W, GT 12EU, CELERON QS QJ4V	071.00BSW.0D0U	BRASWELL 4c FCBGA 1.6GHz 6W , GT 12EU, CELERON QS QJ4T	071.00BSW.0C0U	BRASWELL 4c FCBGA 1.6GHz 6W, GT 16EU, PENTIUM QS QJ4S	071.00BSW.0B0U
eMMC	Hynix/32G	J6PD1	Hynix/32G	J6PD1	SanDisk/32G	4P0NC	Samsung/32G	N8DV6
	SKU7		SKU8		SKU9			
CPU	BRASWELL 2c FCBGA 1.6GHz 6W, GT 12EU, CELERON QS QJ4V	071.00BSW.0D0U	BRASWELL 2c FCBGA 1.6GHz 6W, GT 12EU, CELERON QS QJ4V	071.00BSW.0D0U	BRASWELL 4c FCBGA 1.6GHz 6W , GT 12EU, CELERON QS QJ4T	071.00BSW.0C0U		
eMMC	Hynix/64G	WF56J	SanDisk/64G	7FDJ	Samsung/64G	67D71		

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**Main Func = Power BTN**

## Power Button & Hall Sensor

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**Main Func = LED**

[24] CHG\_AMBER\_LED# >>>

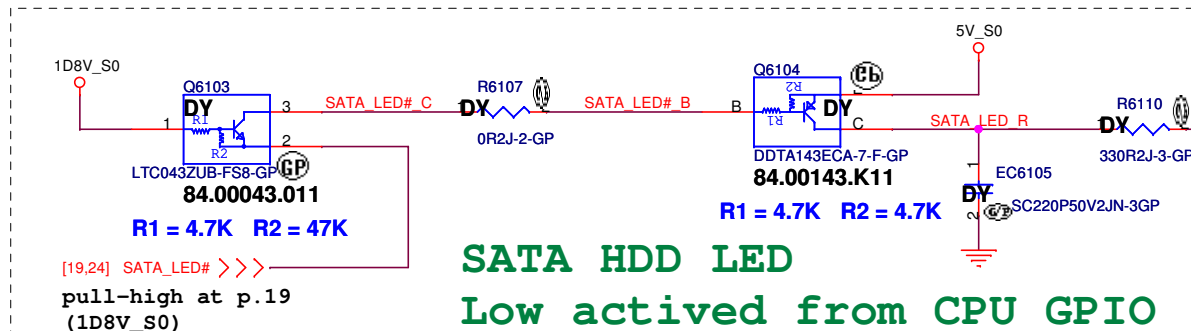
**Battery LED1**

Low actived from KBC GPIO

[24] BATT\_WHITE\_LED# >>>

**Battery LED2**

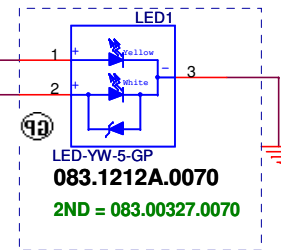
Low actived from KBC GPIO



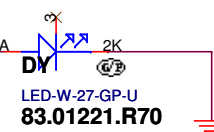
**SATA HDD LED**

Low actived from CPU GPIO

X01



HDLED1



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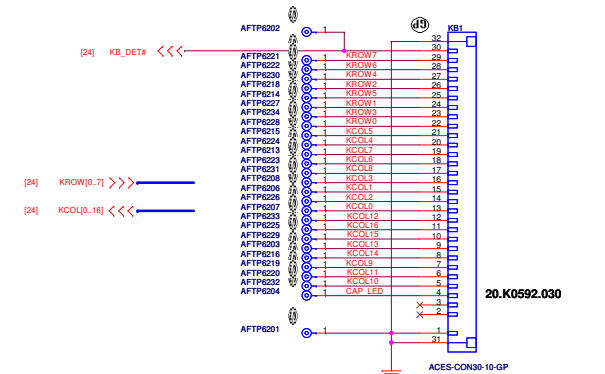
<b>DELL</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>LEDBard/PowerButton</b>			
Size Custom	Document Number <b>Iris BSW</b>	Rev <b>A00</b>	
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Main Func = KB

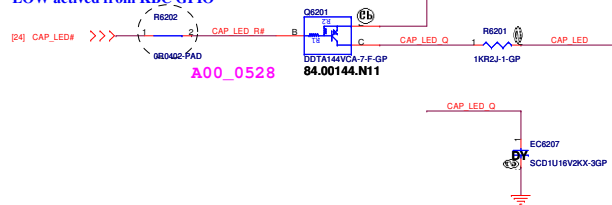
## Keyboard

### Internal Keyboard Connector (14")

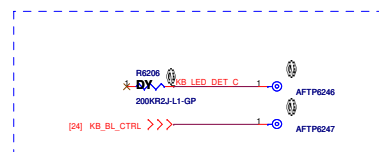


### CAP LED Control

LOW active from KBC GPIO

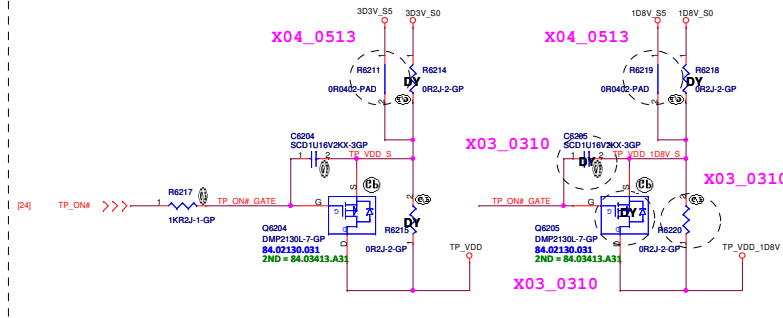


X01

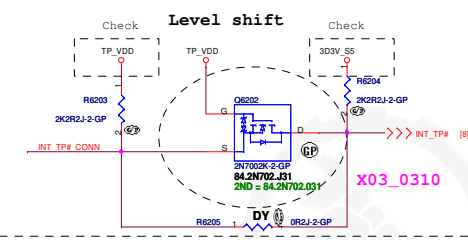


Main Func = TPAD

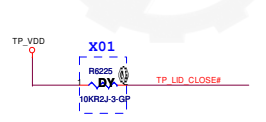
### Touchpad Power



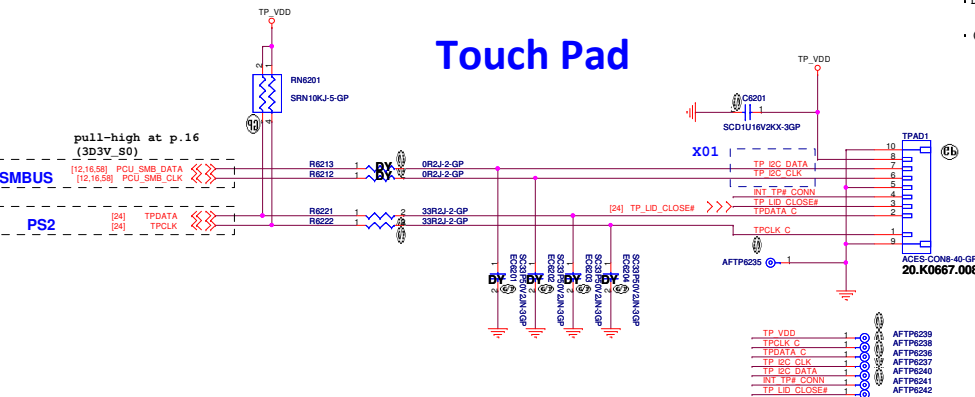
INT#



TP\_LID\_CLOSE#

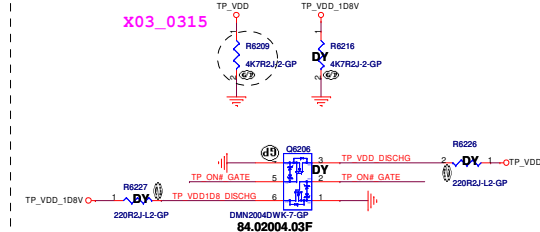


## Touch Pad



### Touchpad Power Discharge

EE Note:  
R6209, R6216, Q6206, R6226, R6227 are for Touchpad discharge.  
Need to confirm the solution base on test result.

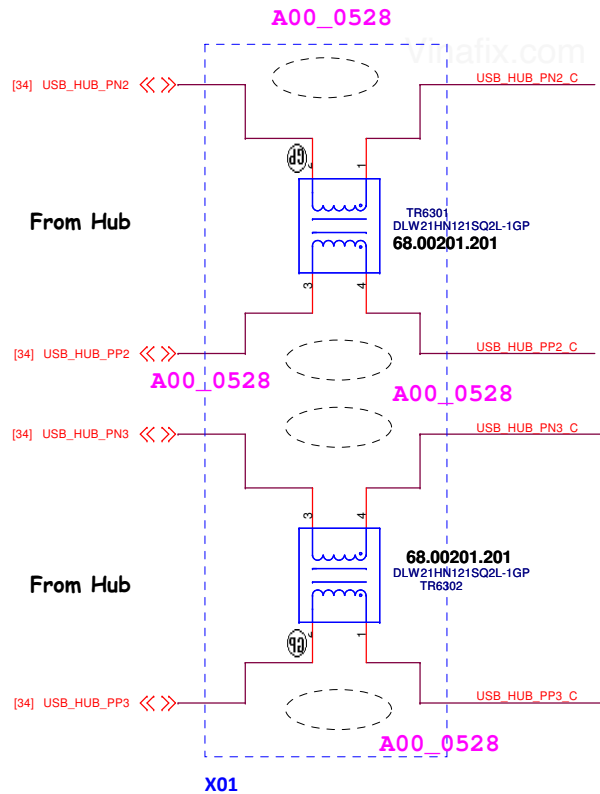


- (#514849) I2C PTP Pins  
Standard I2C pins for interrupt driven I2C device:  
• +3.3V VDD  
• GND  
• SCL (clock)  
• SDA (data)  
• INT# (or INTR#, interrupt), also known as ATTN# (attention)  
-Active low  
Other pins needed on I2C PTP:  
• wake# - level trigger signal from PTP to Host  
-Overload the INTR#/ATTN# line (on the same pin)  
-Only used during S3  
-Active low  
-Connect to either wake capable mechanism on chipset  
• GPIO pin (Suspend Well powered) for S3 platform  
• GPIO on EC (and route to GPIO27 or PWRBTN# on chipset)  
• DSW (interrupt disable)  
-level trigger signal from sensor (late mode decoder) to PTP  
-Active low (active = disable any interrupt, including wake)  
• (Optional) +1.8V VDD

Pin No.	Pin name
1	VDD (3.3V)
2	DAT (I2C)
3	CLK (I2C)
4	GND
5	INT#
6	GPIO
7	DAT (PS2)
8	CLK (PS2)

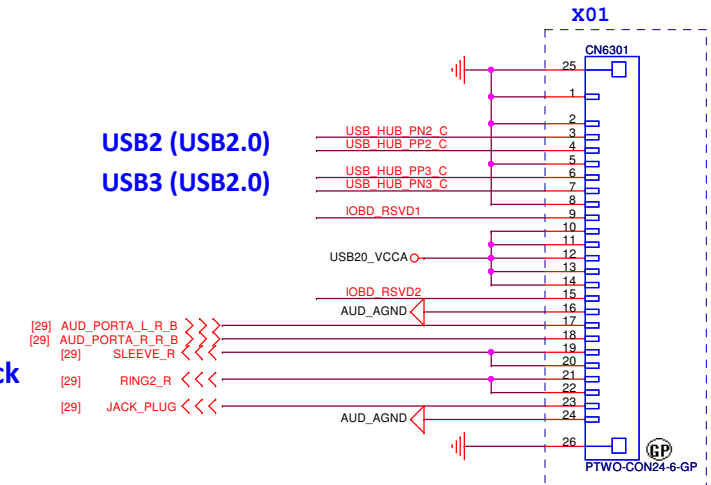
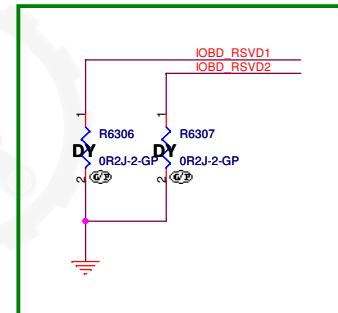
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Main Func = IO Connector



## I/O Board Connector

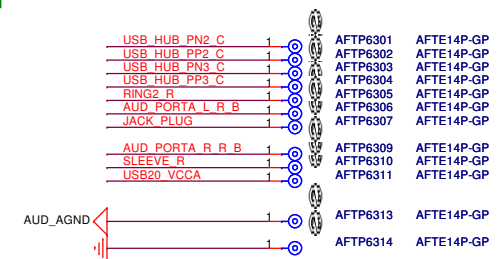
### Universal Jack



MAIN = 020.K0139.0024

2ND = 020.K0095.0024

Pitch: 1mm  
Power: 5 pins  
GND: 4 pins  
AGND: 2 Pins



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IO Board Connector		
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Main Func = Hall Sensor

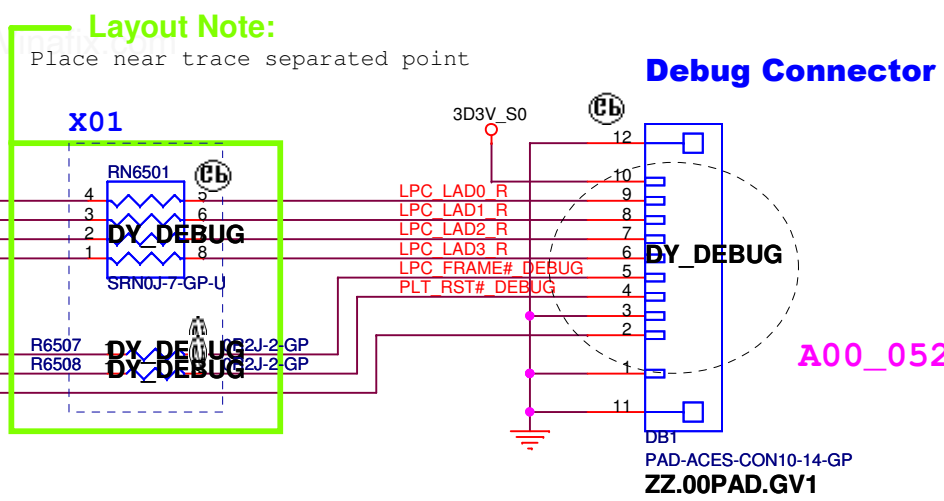
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Main Func = Debug



20.F1180.010: Dummy Pad with solder mask is ZZ.00PAD.GV1

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Title <b>Debug connector</b>			
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Main Func = Sensor Hub+Accelerometer (G-Sensor)+Gyro+Proximity SAR+ALS

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Main Func = G-Sensor

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Main Func = Thunderbolt

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Main Func = Thunderbolt

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Main Func = Thunderbolt

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Main Func = Thunderbolt

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Main Func = Thunderbolt

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Main Func = dGPU

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Main Func = GFXCRT

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Main Func = dGFX\_CORE

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Main Func = GFXLCD

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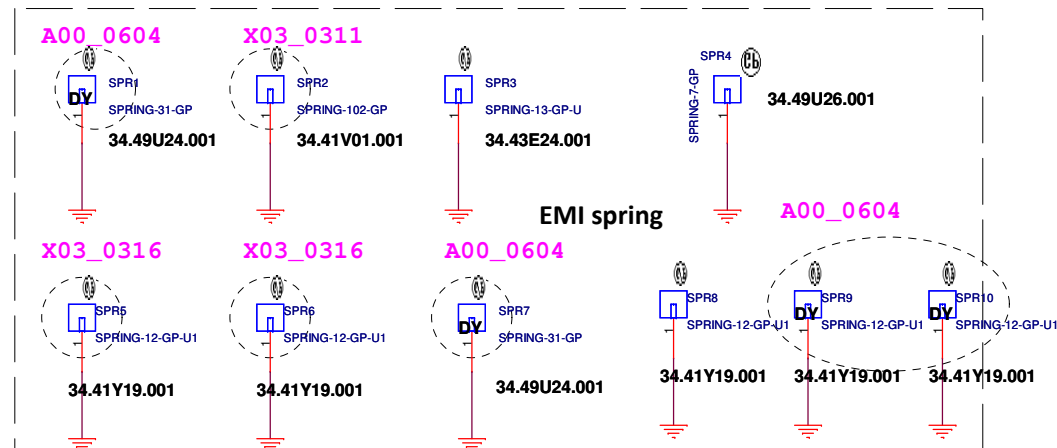
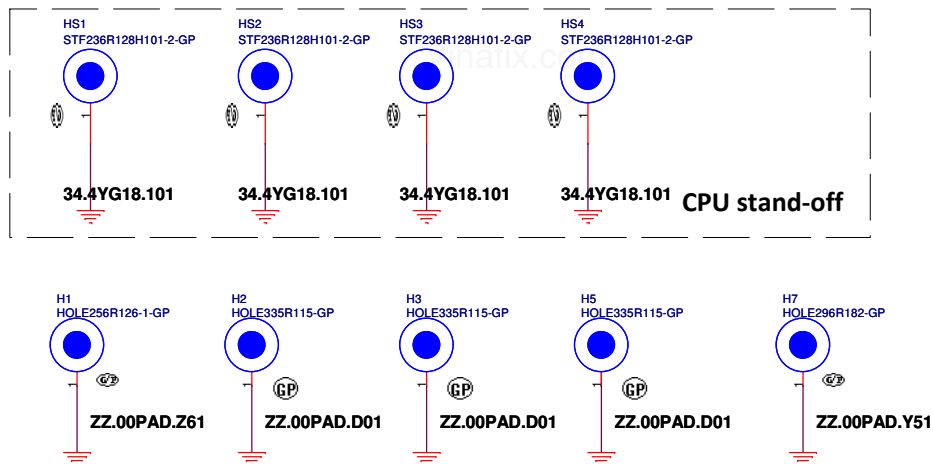
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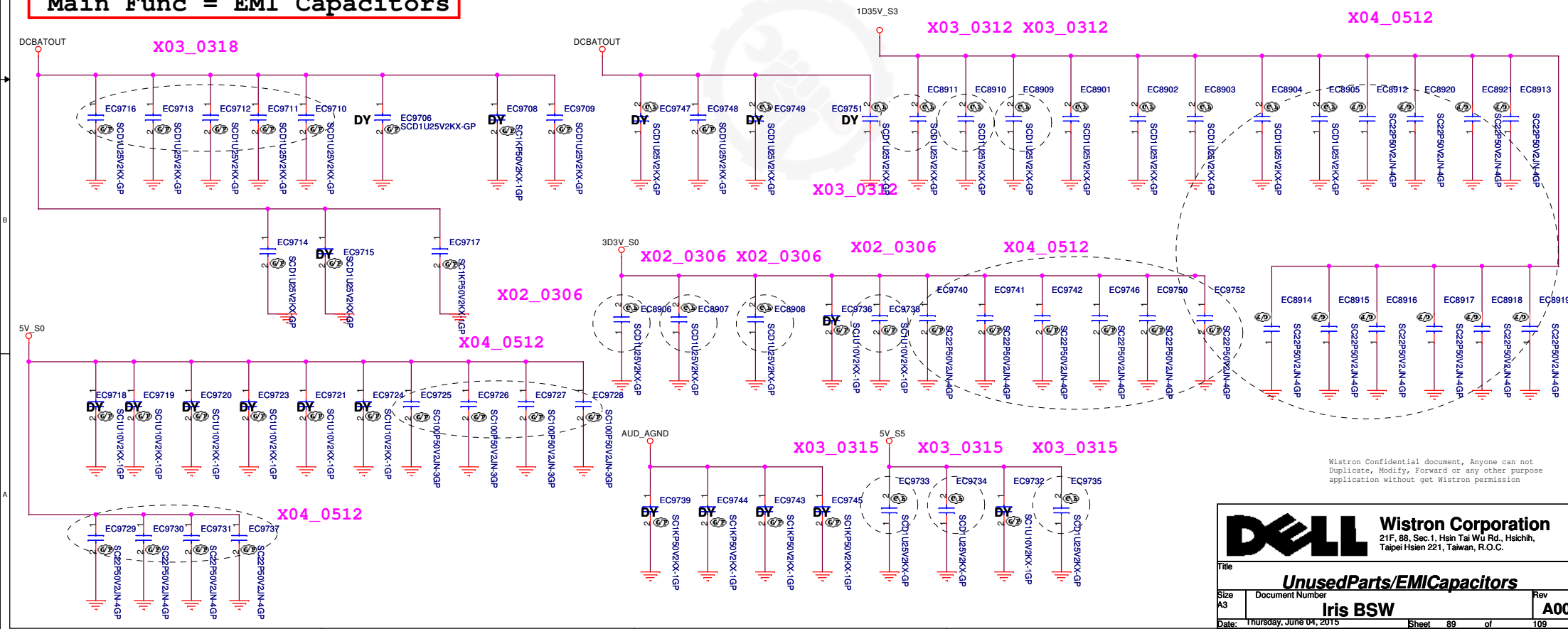
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## Main Func = Unused Parts



## Main Func = EMI Capacitors




Main Func = NFC

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Main Func = TPM

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Main Func = FPR

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Main Func = SmartCard

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Main Func = SmartCard

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Main Func = Switchable

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Main Func = Dock

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Main Func = LAN

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Main Func = LAN

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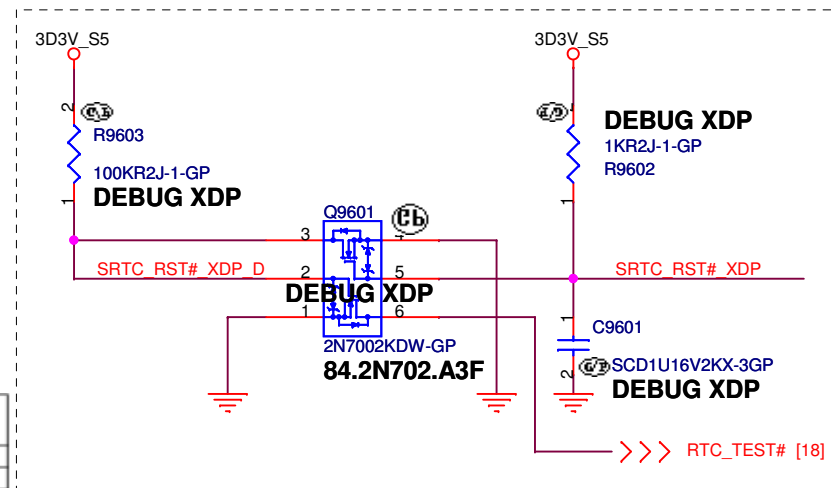
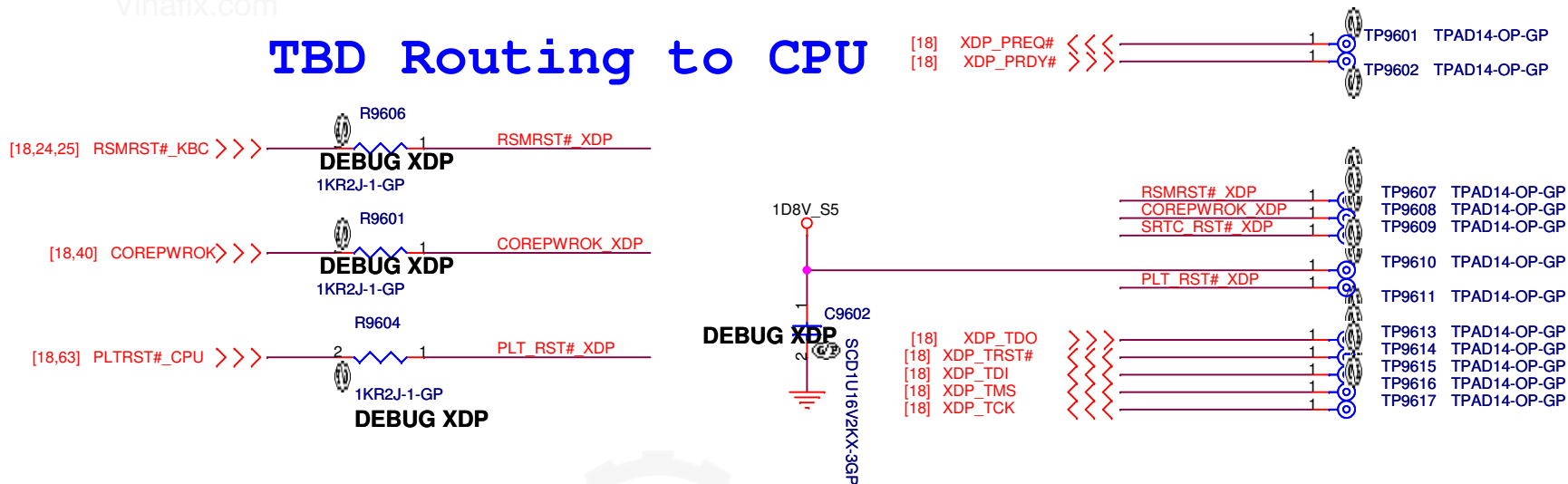
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# SSID = DEBUG PORT

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## TBD Routing to CPU




Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0 <sup>1</sup>	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST# <sup>1</sup>	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4 <sup>1</sup>	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST# <sup>1</sup>	O	System	18	HOOK7	DBR# <sup>1</sup>	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH



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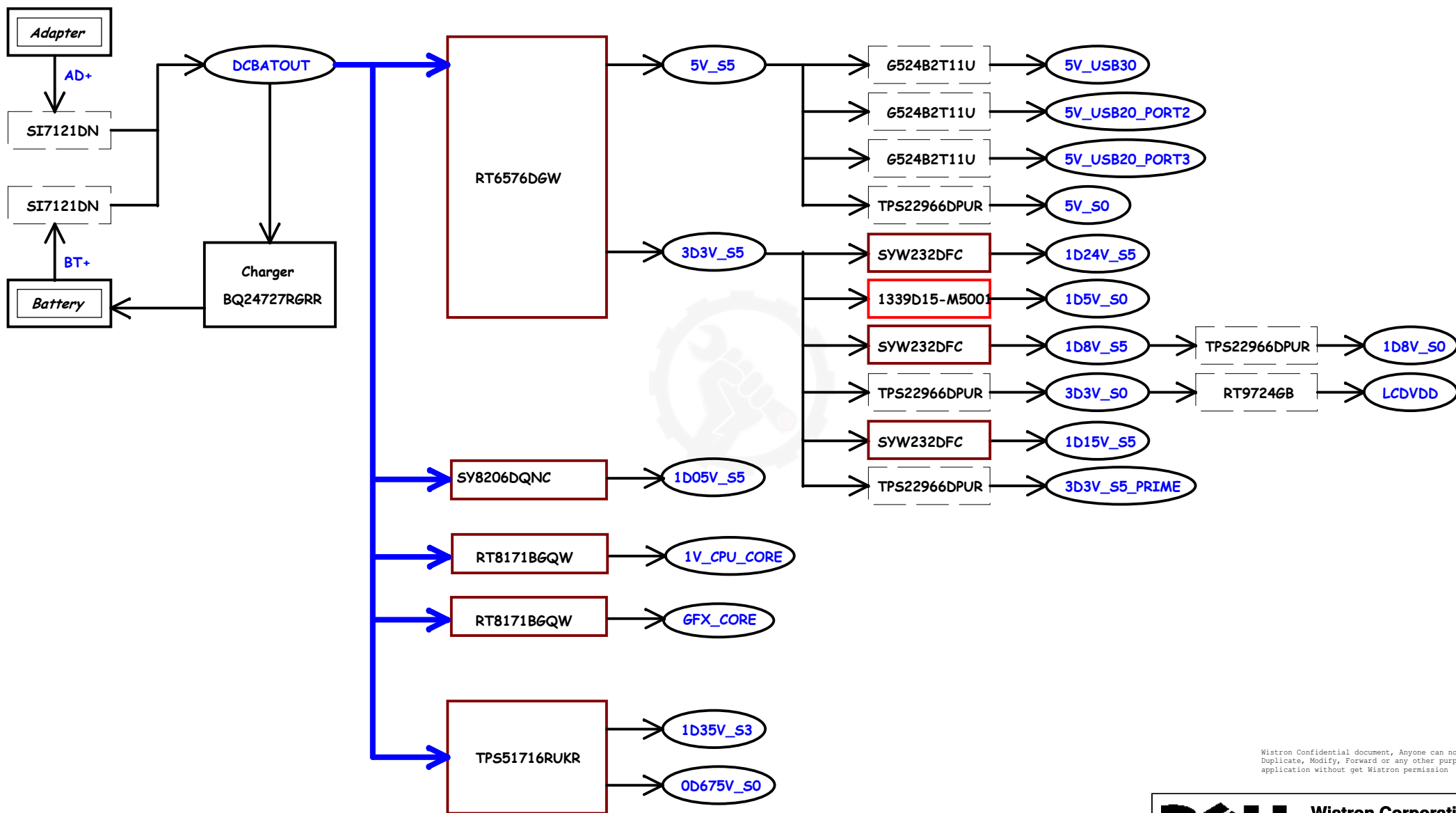
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# Power IC Type

Regulator

LDO

Load  
Switch



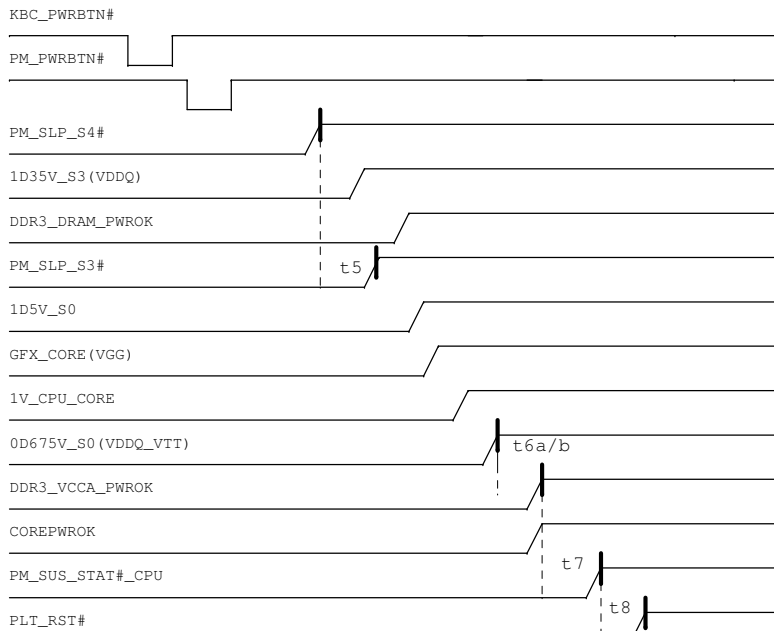
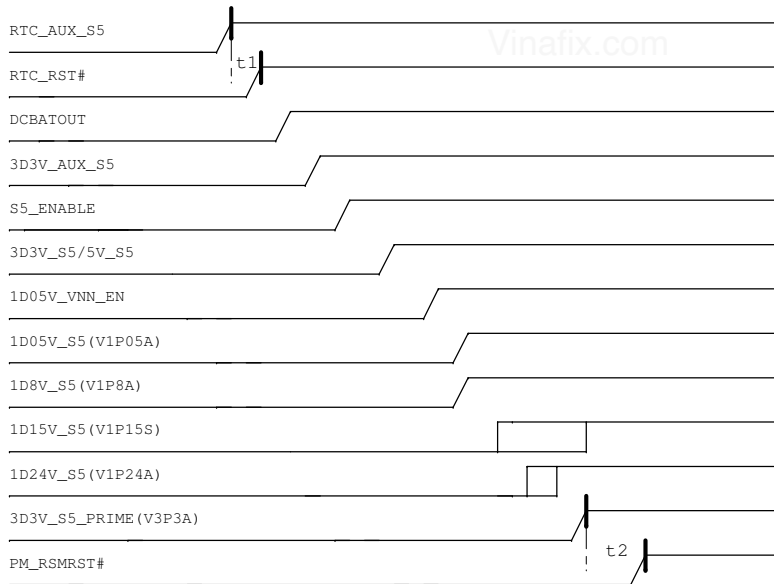
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Power Block Diagram		
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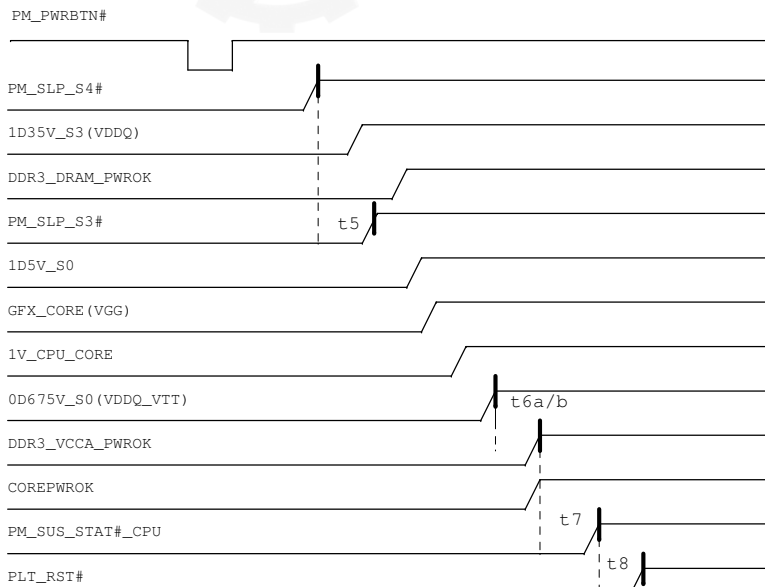
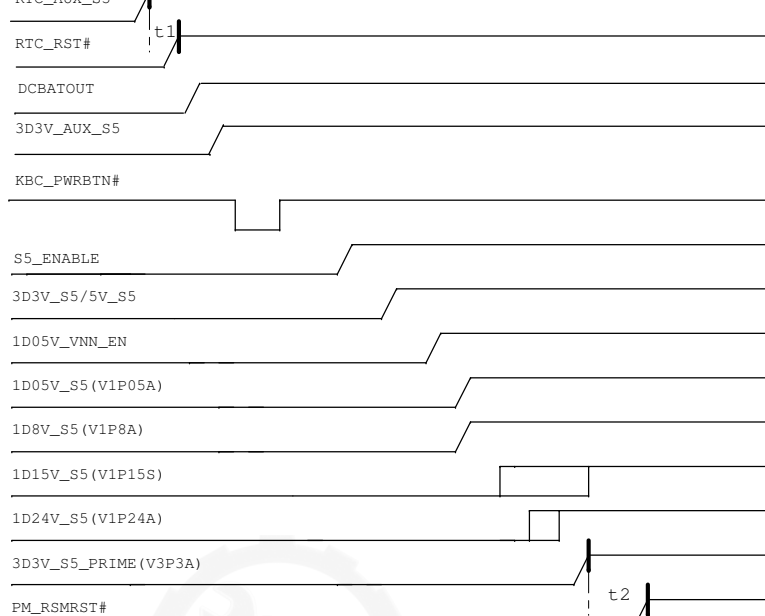
# Intel-Power Up Sequence

(AC mode)



# Intel-Power Up Sequence

(DC mode)

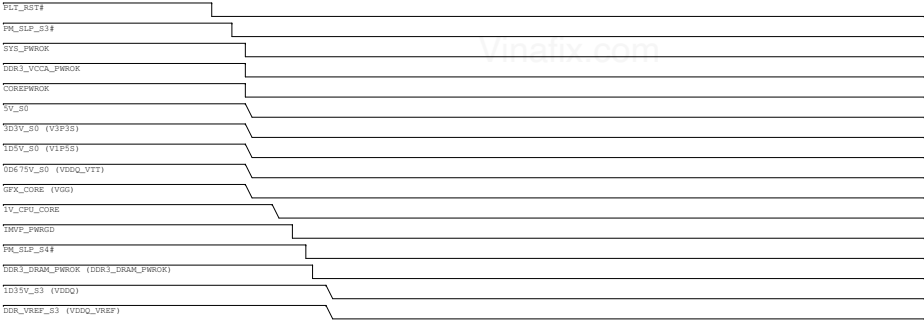


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<b>Power Up Sequence</b>			
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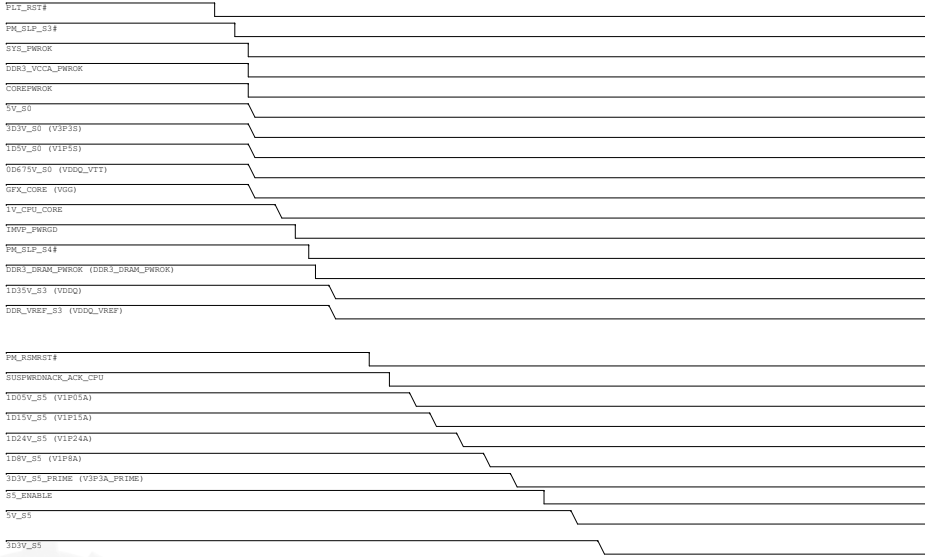
Intel-Power Down Sequence

(AC mode)

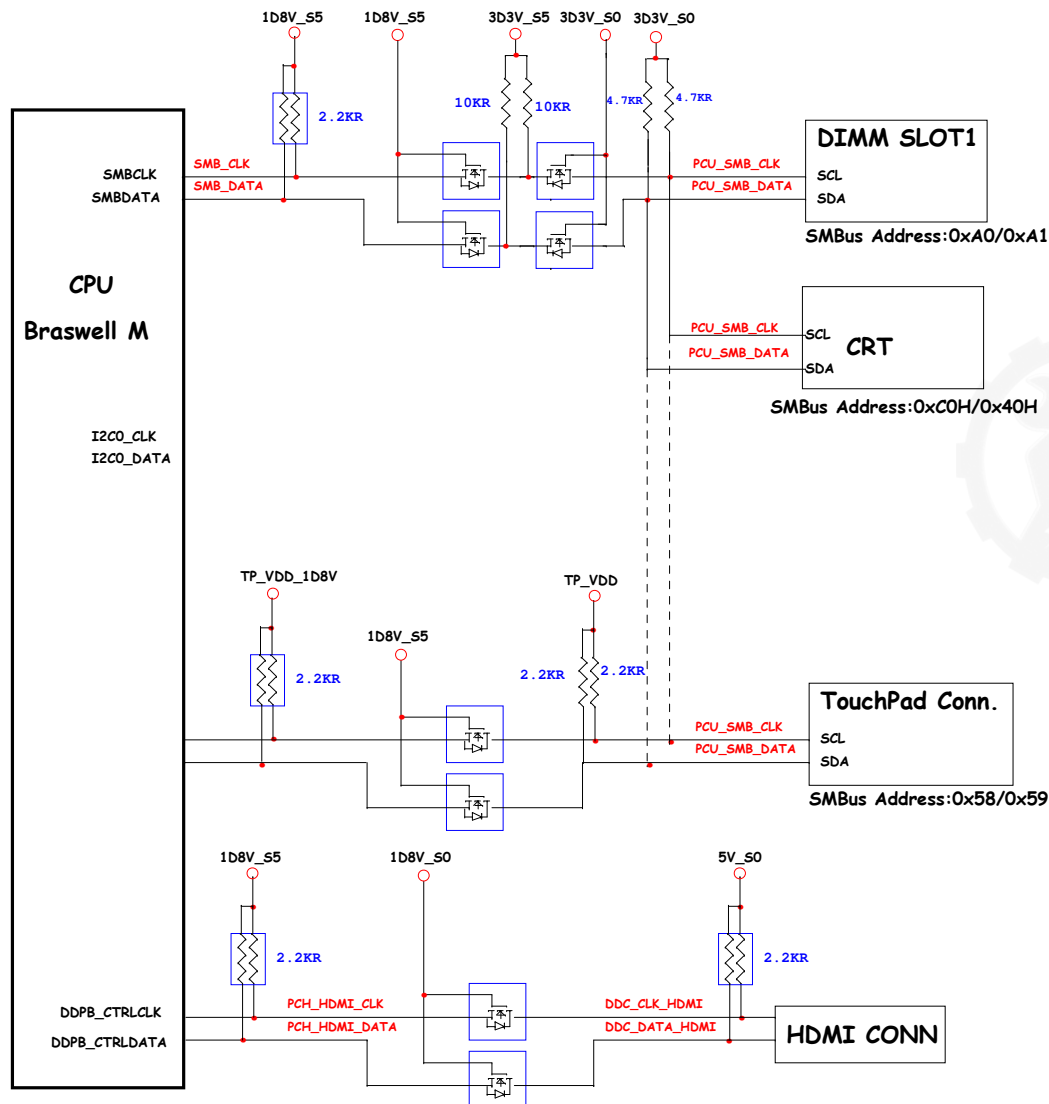


Intel-Power Down Sequence

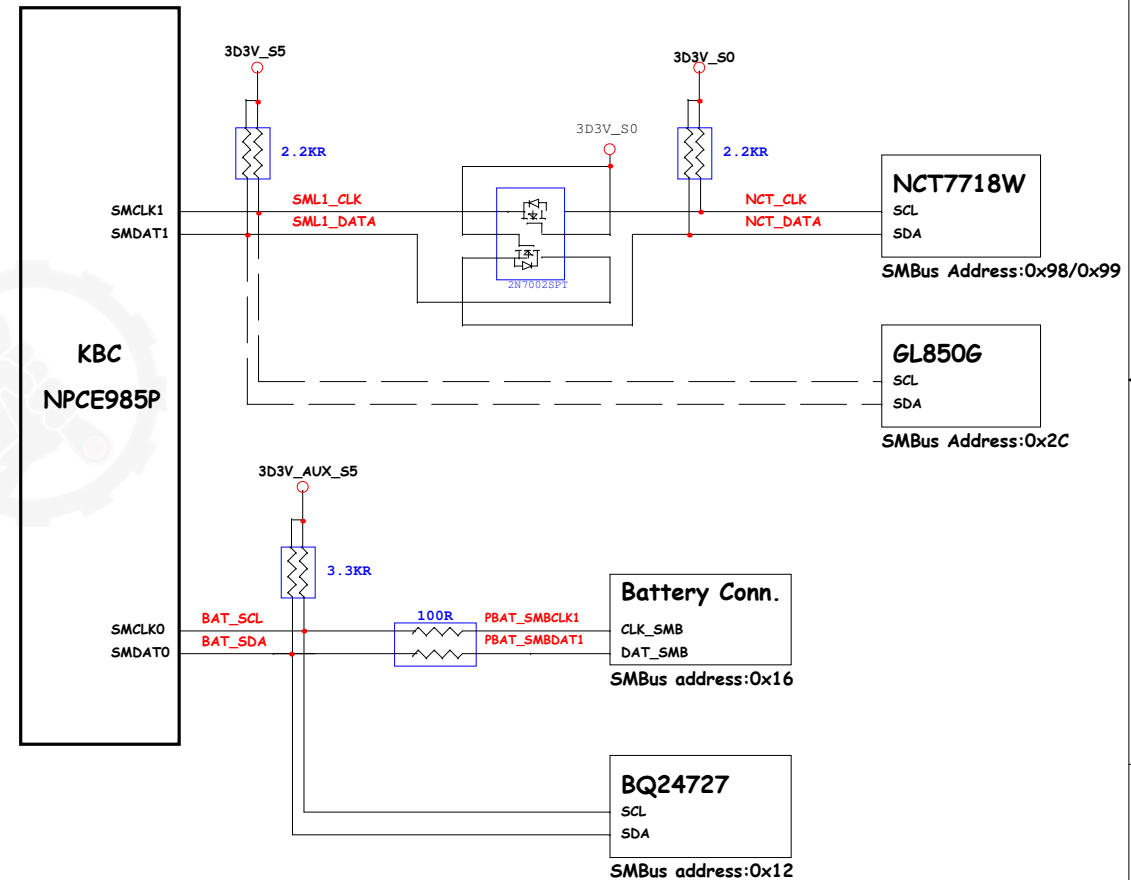
(DC mode)



## CPU SMBus / I2C Block Diagram



## KBC SMBus Block Diagram



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[illegible]

The diagram illustrates the ALC3234 codec's connections to external components. On the left, the codec is represented by a black box with the text "Codec" and "ALC3234" in red. The connections are as follows:

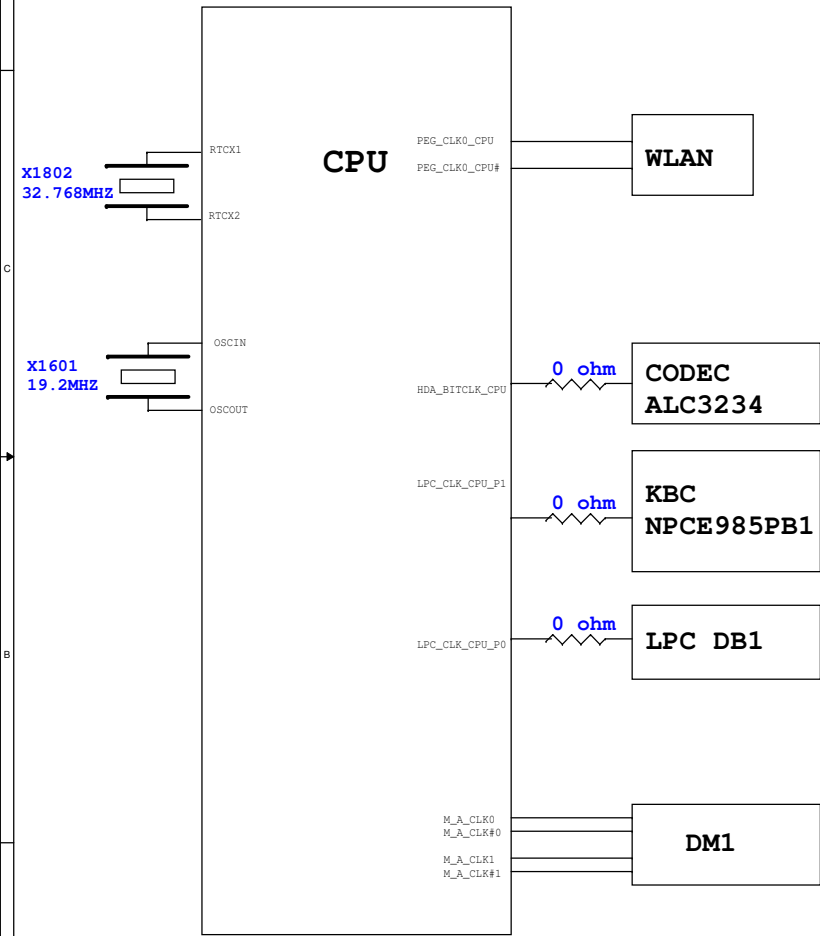
- SPEAKER Connections:**
  - SPK-OUT-L- and SPK-OUT-L+ connect to a "SPEAKER" box.
  - SPK-OUT-R- and SPK-OUT-R+ connect to another "SPEAKER" box.
- HP OUT Connections:**
  - HPOUT-L/PORT-T-L and HPOUT-R/PORT-T-R connect to the "HP OUT" box through resistors.
  - MIC2-L/PORT-F-L and MIC2-R/PORT-F-R connect to the "HP OUT" box through a capacitor and resistors.
  - SENSE\_A connects to the "HP OUT" box through a resistor.
- MIC IN Connections:**
  - DMIC\_CLK and DMIC\_DAT connect to the "MIC IN" box through resistors.

DELL

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SSID = CLK Block Diagram

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<Core Design>


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Date	Page	Change Notice	Ver.	Date	Page	Change Notice	Ver.
2014/9/25	99	Del XDPI, Change to TP	X00	2014/10/3	21,24	1. Keep reserve R2101, R2102,R2103(DY) 2. Keep reserve MODEL_ID_AD PUPD Resis.	X00
2014/9/26	16	CFG0~8 add Test point	X00	2014/10/6	21	CPU2 change location to CPU1	X00
2014/9/26	8	GP_CAMERASB00~07 add Test point	X00	2014/10/6	99	Remove R9605 and C9603	X00
2014/9/26	99	DBG0~3 add test point	X00	2014/10/6	19	Separate RN1901 and change R1901 to 10K ohm	X00
2014/9/26	54	Change PG5408, PG5409 to close gap	X00	2014/10/6	24	Reserve 10k PU (DY) to 1D8V_S0 on LPC_SERIRQ_CPU	X00
2014/9/26	10,42-54	Update PWR team PWR Cape and PWR team circuit PG42-54	X00	2014/10/6	8,16	DBC_EN_C move to CPU ballout F2 (Follow Redwood)from GPIO review	X00
2014/9/30	45,48	PWR team modify items: 1.PR4841~4.42K 2. PR4801~360ohm 3. PR4840~3.4K 4.PR4517~140K	X00	2014/10/6	18,24,40	Del PCH_PCIE_WAKE#, 3D3V_S5_PRIME_PG, SIO_SLP_S0IX# from GPIO review	X00
2014/9/30	18,48,57,60,89	1. HDMI change to ZZ PN for co-layout with CRT. 2. Add G1802 for RTC reset 3.Follow ME EMN to update HDD1, H51~4 4.Delete PT4802, And add one more PT4801	X00	2014/10/6	8	INT_TP# Move to SDMMC3_D1 from SW review	X00
2014/10/1	10,48	1. PG10 PWR CAP (All of cap to mounted) 2. PT4802 change to DY	X00	2014/10/6	10,11	Delete the 10 caps for increasing via space (As black cycle)	X00
2014/10/1	15	Stuff R1522 and DY R1523 because "ICLK, USB2, DDI SFR Supply Select" is 1.24V	X00	2014/10/7	8,16	EC_SWI# move to SDMMC2_D0	X00
2014/10/1	11,16,18,62	1. R6204 change to Dummy,Q6202. Gate change to 1D8V_S5 2. Update RTC RESET circuit 3. Add Page11 PWR cap. 4. Del 19.2MHZ series Resis. 5. Change R1613, R1614, C1609 to mounted for USB_VBUSSENS	X00	2014/10/7	19	Del R1905,R1902,Q1901, Reserve series 0ohm R1904.(DY) between PEG_CLKREQ0_CPU# and PEG_CLKREQ0_WLAN#	X00
2014/10/1	57	change PU HDMI_CRT_DET to 1D8V_S5	X00	2014/10/7	24	KBC Pin25 (GPIO50) wire to RUNPWROK, KBC pin100 (GPIO93) wire to KB_DET# and reserve R2466(DY) PU 1D8V_S0	X00
2014/10/1	18	Del R1823 for SVID	X00	2014/10/7	18	Q1814,Q1815 remove, reserve R1832(DY) PH 1D8V_S5 on PM_SLP_S0IX# (follow BTM)	X00
2014/10/2	18,19,27,99	1. Q1801 change main source for reduce source amount 2. DY S0IX Fun. Parts (4PCS) R1832, R1836, Q1814, Q1815 3. Del R1823 (SVID CLK) 4. Follow Redwood LVDS_VDD_EN_CPU circuit(DY) 5. Follow Redwood reserve R2710(DY), R2712(DY) (vendor suggestion) 6. C2702 change to 10Uf (vendor suggestion) 7. R1845 Dummy follow Redwood 8. Reserve R1905(DY) PU 1D8V_S0 for WLAN PEG_CLKREQ0_CPU# 9. Q9601.6 change to RTC_TEST# 10. SPI Routing follow Redwood	X00	2014/10/7	8,96	Del DBG test point TP804~807, TP9603~06	X00
2014/10/2	19,52,64,24,25	1. C5201, C5205 change to 0.1UF 2. SATA_LED# Add R1906(10K) PU to 1D8V_S0 3. Del PWR button, Add G6401, G6402 4. Add 128Kbyte SPI ROM for KBC 5. DY resistors from share ROM to KBC (Dummy R2515, R2517, R2511, R2510)	X00	2014/10/7	89	Del EC9710---etc EMI parts	X00
2014/10/2	18,45	1. R1826 change to mounted 2. PR4534 change to Dummy	X00	2014/10/7	21	Del R2107~R2110 and R2118 for saving layout space	X00
2014/10/3	18,24,37,45	1. DY R2412, R2407, R2402 2. U2401.2 Net name should be EC_SPI_S0_FLASH and connect to KBC24.86 through 33R. 3. U2401.5 net name should be EC_SPI_S1_FLASH and connect to KBC87 through 33R. 4. Change 13" reel parts to 7" parts 5. R1826 change to mounted 6. PR4534 change to Dummy 7. R3705 to mounted, R3701 DY	X00	2014/10/7	10	Add PC1002, PC1003	X00
2014/10/3	19,21,24,36,40,61	1. modify U3701.6 and U3701.7 to 3D3V_S5. 2. Modify "1D35V_S0_EN" to "3D3V_S5_PRIME_EN". 3. WLAN change to PCIe pair0 (Follow Redwood) for SW saving Pair1~3 power	X00	2014/10/7	24	Del 1D8V_S5_PG	X00
		1. Reserve TP2101 (Follow Redwood and CDD)		2014/10/7	24	Reserve 3D3V_S5_PRIME_PG to KBC GPIO54	X00
				2014/10/7	40	Del D3V_S5_PRIME series resistor R3628(DY)	X00
				2014/10/7	24	EC_VTT(1.05V) add R2462 for division circuit	X00
				2014/10/7	Net swap sheet	USB/CAMERA Choke swap as Net swap sheet	X00
				2014/10/7	66	Change TR6301, TR6302 source (Follow BTM)	X00
				2014/10/7	40	Del 1D05V_S0 discharge circuit and change Q3610 source(Follow Redwood)	X00
				2014/10/7	54	PC5401 change to 78.10523.2BL	X00
				2014/10/8	52	1.DY PR5202 and PC5225 for adjust the 1.8V sequence before 1.15V (Follow Plano BSW) 2.Add 1D05V_VNN_PWRGD to PWR_1D8V_S5_EN by 0 ohm(Follow Plano BSW)	X00
				2014/10/8	54	DY PR5401. (PWR_1D15V_PG PH to 3D3V_S5 by PR5012, will have leakage about 0.058mA (3.3V/57K ohm) if stuff PR5401(Follow Plano BSW).	X00
				2014/10/8	16	Remove R1602 because there is already R1506 for SOC_RUNTIME_SC1#	X00
				2014/10/8	24	DY the resistor R2466 and change R2466.1 to 3D3V_S0.	X00
				2014/10/8	65	DY R6214,R6218, ASM R6211, R6219 for Touch PAD Power rail	X00
				2014/10/8	18	R1861 change to 63.10434.1DL Follow Redwood	X00
				2014/10/8	61	DY R815 for no-using PEG_CLKREQ0_WLAN#	X00
				2014/10/8	50	Add PR5040, PR5039 change to 10ohm for 1D05V power team update	X00
				2014/10/8	8	DBC_EN_C move to CPU ballout D2 (Follow Redwood)from GPIO review	X00
				2014/10/8	24,25	Add property DY_Share(honS: Share ROM(Dummy) or Non Share ROM	X00
				2014/10/9	89	Remove EC9713, Ec9705, Ec9713, Ec9702	X00
				2014/10/9	40	Remove 3D3V_S5_PRIME power good circuit, reserve RC delay circuit to KBC. To increase spacing for CPU decoupling caps and vias.	X00
				2014/10/9	61	Change WLAN1 to 062.10007.0081 base on the latest EMN.	X00
				2014/10/9	40,54	Reserve PWR_1D24V_POK to 3D3V_S5_PRIME_EN.	X00
				2014/10/9	10	[Power/Alan] Add PC1013 on 1V_CPU_CORE and PC1014 on GFX_CORE.	X00
				2014/10/9	19	Reserve DEVSLP circuit for HDD.	X00
				2014/10/9	7	Remove TP701 to increase space for CPU power.	X00
				2014/10/9	24	Reserve SUSPWRDNACK_SOC_EC on KBC GPIO84	X00
				2014/10/9	89	[ME/Will] Add SPR4 34.49U26.001.	X00
				2014/10/11	8	Change DBC_EN_C to SDMMC3_CLK (follow Redwood BSW).	X00
				2014/10/13	9	Change CPU1.B52 to NC because Layout cannot breakout. (Follow Redwood BSW and Plano BSW)	X00
				2014/10/13	Net Rule	[Power/Alan] Modify VSS_VNN_SENSE spacing to 10 mil.	X00
				2014/10/14	50	[Power/Alan] PR5011 change to 64.95325.6DL	X00
				2014/10/14	55	[Layout/Connie] RN5201.4 and RN5201.1 + RN5201.5 and RN5201.8 swap	X00
				2014/10/15	66	[ME/Will] Update CN6301 (20.K0610.024-> 20.K0846.024)	X00
				2014/10/16	58	R1627 & R1647 改用 4.7K	X00
				2014/10/16	60	EC512 0. 1C5207 換裝 33K 10K 47K 100K	X00


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